83322320

CONTROL DATA CORPORATION

CDC® STORAGE MODULE DRIVE

BK6XX

BK7XX

GENERAL DESCRIPTION

OPERATION

THEORY OF OPERATION

DISCRETE COMPONENT CIRCUITS

HARDWARE REFERENCE MANUAL

REVISION RECORD

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PREFACE

This manual contains reference information applicable to Control Data BK6XX/BK7XX Storage Module Drives (SMD's).

The specific types of drives covered and their configuration are listed on the Configuration Chart (refer to table of contents).

Most of the information in this manual is applicable to all types of the above drives. However, where information is applicable to only specific types, this is noted in the text.

The manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the storage module drive (SMD).

Reference information is provided in six sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - General Description. Describes equipment functions, specifications, and equipment number identification.

Section 2 - Operation. Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation. Describes basic logic and mechanical functions.

Section 4 - Description of discrete components and their functions. For ease of using the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section, arranged in alphabetical order of the circuit type designator (AAA-ZZZ) explains these functions and illustrates the actual discrete elements.

Manuals applicable to the previously listed BK6XX/BK7XX SMD's.

Publication No.	Title
83322310	Hardware Maintenance Manual
83322320	Hardware Reference Manual
83322440	Normandale Circuits Manual

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FIGURES

TABLES

CONFIGURATION CHART

EQUIP-MENT	*** INPUT VOLTAGE		** STANDARD OPTIONS				TLA* Number	Color Code
	208 v 60 Hz	220 v 50 Hz	A Cable I/O	Dual Channel	Index & Sector Con-figuration	Pack Access Cover Solenoid		
BK6A1A	X		60-pin		S&I0AC		77456102	A
BK6A1B		X	60-pin		S&I0AC		77456103	A
BK6A1D		X	60-pin		S&I0AC		77456120	G
BK6A1E	X		60-pin		S&I0BC		77456121	L
BK6A1F		X	60-pin		S&I0BC		77456122	L
BK6A1G	X		60-pin		S&I0AC		77456125	S
BK6A1H		X	60-pin		S&I0AC		77456126	S
BK6A2A	X		60-pin	Yes	S&I0AC		77456104	A
BK6A2B		X	60-pin	Yes	S&I0AC		77456105	A
BK6A4A	X		60-pin	Yes	S&I0BC		77456116	
BK6A4B		X	60-pin	Yes	S&I0BC		77456117	
BK6A4C	X		60-pin		S&I0BC		77456118	C
BK6A4D		X	60-pin		S&I0BC		77456119	C
BK6A5A	X		50-pin	Yes	S&I0AC		77456112	A
BK6A5B		X	50-pin	Yes	S&I0AC		77456113	A
BK6A5C	X		50-pin		S&I0AC		77456114	A
BK6A5D		X	50-pin		S&I0AC		77456115	A
BK6A9A	X		60-pin	Yes	S&I0AC		77456108	
BK6A9B		X	60-pin	Yes	S&I0AC		77456109	
BK6A9C	X		60-pin		S&I0AC		77456110	B
BK6A9D		X	60-pin		S&I0AC		77456111	B
BK7A1A	X		60-pin		S&I0AC		77456002	A
BK7A1B		X	60-pin		S&I0AC		77456003	A
BK7A1D		X	60-pin		S&I0AC		77456028	G
BK7A1E	X		60-pin		S&I0AC		77456029	H
BK7A1F		X	60-pin		S&I0AC		77456030	H
BK7A1G	X		60-pin		S&I0AC		77456031	J
BK7A1H		X	60-pin		S&I0AC		77456032	J
BK7A1J	X		60-pin		S&I0BC	Yes	77456033	K
BK7A1K		X	60-pin		S&I0BC	Yes	77456034	K
BK7A1L	X		60-pin		S&I0AC		77456037	⚠1
BK7A1M		X	60-pin		S&I0AC		77456038	⚠1
BK7A1N	X		60-pin		S&I0BC		77456039	L
BK7A1P		X	60-pin		S&I0BC		77456040	L
BK7A1R	X		60-pin		S&I0AC		77456043	M
BK7A1S		X	60-pin		S&I0AC		77456045	M
BK7A1T	X		60-pin		S&I0AC		77456046	N

* For factory use only.

** Defined under Equipment Configuration in section 1 of this manual.

*** 208 Volt, 60 Hz drives can be rewired for 230 Volt, 60 Hz and 220 Volt, 50 Hz drives can be rewired for 240 Volt, 50 Hz. See Installation Section in Maintenance Manual.

⚠1 Unit has Special Manual Supplement.

Table Continued on next page

CONFIGURATION CHART (CONTD)

EQUIPMENT	*** INPUT VOLTAGE		** STANDARD OPTIONS				*TLA Number	Color Code
	208 V 60 Hz	220 V 50 Hz	A Cable I/O	Dual Channel	Index & Sector Configuration	Pack Access Cover Solenoid		
BK7A1U		X	60-pin		S&I0AC		77456048	P
BK7A1V	X		60-pin		S&I0AC		77456047	P
BK7A1Y	X		60-pin		S&I0AC		77456049	S
BK7A1W		X	60-pin		S&I0AC		77456050	S
BK7A1Z		X	60-pin		S&I0AC		77456051	T
BK7A2A	X		60-pin	Yes	S&I0AC		77456004	A
BK7A2B		X	60-pin	Yes	S&I0AC		77456005	A
BK7A2C	X		75-pin	Yes	S&I0AC		77456044	R
BK7A2D	X		75-pin	Yes	S&I0BC	Yes	77456053	V
BK7A2E		X	75-pin	Yes	S&I0BC	Yes	77456054	V
BK7A2G	X		75-pin	Yes	S&I0ABC		77456062	⚠1
BK7A2H		X	75-pin	Yes	S&I0ABC		77456063	⚠1
BK7A5A	X		60-pin	Yes	S&I0BC	Yes	77456012	D
BK7A5B		X	60-pin	Yes	S&I0BC	Yes	77456013	D
BK7A5C	X		60-pin		S&I0BC	Yes	77456014	D
BK7A5D		X	60-pin		S&I0BC	Yes	77456015	D
BK7A6A	X		50-pin	Yes	S&I0AC		77456016	A
BK7A6B		X	50-pin	Yes	S&I0AC		77456017	A
BK7A6C	X		50-pin		S&I0AC		77456018	A
BK7A6D		X	50-pin		S&I0AC		77456019	A
BK7A7A	X		60-pin	Yes	S&I0BC		77456020	
BK7A7B		X	60-pin	Yes	S&I0BC		77456021	
BK7A7C	X		60-pin		S&I0BC		77456022	C
BK7A7D		X	60-pin		S&I0BC		77456023	C
BK7A8A	X		60-pin		S&I0BC		77456024	E
BK7A8B		X	60-pin		S&I0BC		77456025	E
BK7A9A	X		60-pin		S&I0AC		77456008	
BK7A9B		X	60-pin		S&I0AC		77456009	
BK7A9C	X		60-pin		S&I0AC		77456010	B
BK7A9D		X	60-pin		S&I0AC		77456011	B
BK7A9E	X		50-pin		S&I0AC		77456026	F
BK7A9F		X	50-pin		S&I0AC		77456027	F
BK7B1A	X		50-pin		S&I0AC		77456052	U
BK7B1C	X		50-pin	Yes	S&I0AC	Yes	77456055	V
BK7B1D		X	60-pin	Yes	S&I0BC	Yes	77456056	V
BK7B1G	X		75-pin		S&I0ABC		77456060	⚠1
BK7B1H		X	75-pin		S&I0ABC		77456061	⚠1

* For factory use only.

** Defined under Equipment Configuration in section 1 of reference manual.

*** 208 Volt, 50 Hz drives can be rewired for 230 Volt, 60 Hz and 220 Volt, 50 Hz drives can be rewired for 240 Volt, 50 Hz. See Installation section for instructions.

⚠1 Unit has Special Manual Supplement.

SECTION 1

GENERAL DESCRIPTION

GENERAL DESCRIPTION 1

INTRODUCTION

The Control Data BK6XX and BK7XX Storage Module Drives (SMD's) are high speed, random access digital data storage devices that connect to a central processor through a controller. The major difference between the BK6XX and BK7XX is in their data storage capacity. The total data storage capacity of the BK6XX is 150 megabytes and BK7XX is 300 megabytes. All the equipment specifications for each drive are listed in table 1-1.

The remainder of this section provides a general description of the drive and is divided into the following areas:

- Drive Functions - Explains the major functional areas of the drive.
- Drive Physical Description - Provides description of the drives physical characteristics.
- Equipment Configuration - Describes the various drive configurations and how to identify them.

TABLE 1-1. EQUIPMENT SPECIFICATIONS

Specification	Value
Size	
Height	36 in (920 mm)
Width	36 in (914 mm)
Depth	23 in (584 mm)
Weight	550 lbs. (252 kg)
Temperature	
Operating	59^{o} F (15.5^{o} C) to 90^{o} F (32.2^{o} C)
Operating Change/Hr	12^{o} F (6.6^{o} C) per hr
Transit (packed for shipment)	-40^{o} F (-40.4^{o} C) to 158^{o} F (70.0^{o} C)
Non-Operating Change/Hr	36^{o} F (20^{o} C) per hr
Relative Humidity	
Operating	20% to 80% } No Condensation
Transit (packed for shipment)	5% to 95% }
Altitude	
Operating	-1000 ft (305 m) to 6500 ft (2000 m)
Transit (packed for shipment)	-1000 ft (305 m) to 15,000 ft (4572 m)
Disk Pack	
Type	883-91 (one per drive)
Disks/Pack	12 (Top and bottom disks are for protection only.)
Data Surfaces	19
Servo Surfaces	1
Usable Tracks/Surface	823 (150 MB units use only 411 of these tracks)
Tracks/Inch	384
Track Spacing (center to center)	.0026 (.066 mm)
Coating	Magnetic Oxide
Data Capacity	150 MB / 300 MB (NOTE: Based on 8 bit bytes not allowing for tolerance gaps for sectoring etc.)
Bytes/Track	20 160 / 20 160
Bytes/Cylinder	383 040 / 383 040
Bytes/Spindle	154 748 160 / 309 496 320
Cylinders/Spindle	411 / 823

Table continued on next page

TABLE 1-1. EQUIPMENT SPECIFICATIONS (Cont'd)

Specification	Value
Recording Characteristics Mode Density (nominal) Outer Track Inner Track Rate (nominal)	 Modified Frequency Modulation (MFM) 4038 bits/in (1590 bits/cm) 6038 bits/in (2377 bits/cm) 9.67 MHz (1 209 600 bytes/sec)
Heads Read/Write Servo Read/Write Width	 19 1 BK6XX - .004 in (.102 mm) BK7XX - .002 in (.051 mm)
Seek Characteristics Mechanism Max Seek Time (411 or 823 Tracks) Max Track Seek Time Average Seek Time	 Voice Coil, Driven By Servo Loop 55 ms 6 ms 30 ms
Latency Average Maximum	 8.33 ms (at 3600 r/min) 17.3 ms (at 3474 r/min) NOTE: Latency is time required to reach specific track location after drive is on cylinder.
Spindle Speed	3600 r/min
Controllers Per Drive	Refer to Configuration Chart in front matter of this manual
Input Voltages	Refer to Configuration chart in front matter of this manual

DRIVE FUNCTIONAL DESCRIPTION

GENERAL

The major functional areas of the drive are shown on figure 1-1 and described in the following paragraphs. More detailed descriptions of each of the following areas is found in section 3 of this manual (Theory of Operation).

DISK PACK

The disk pack is the recording medium for the drive. The disk pack consists of ten, 14-inch disks, center mounted on a hub. The recording surface of each disk is coated with a layer of magnetic oxide and related binders and adhesives.

There are nineteen recording surfaces and one servo surface. The servo surface contains prerecorded information that is used by the servo circuits to position the heads at the desired area on the disk pack.

The recording surfaces are used for data storage. Each of these surfaces has its recording tracks grouped in a 2 inch band near the outer edge of the disk. The number of tracks contained on each recording surface and the spacing between the tracks is found in table 1-1.

The disk pack is portable and is interchangeable between drives. Both the BK6XX and BK7XX use the same type of disk pack.

POWER SYSTEM

The drive has its own self contained power supply which receives its input from the site main power source. The power supply provides all the voltages necessary for drive operation.

INTERFACE

The drive can communicate only with the controller. The controller issues all commands to the drive, which decodes the commands and initiates the proper operation. In addition to the commands, the controller sends write data, write clock and power sequence information to the drive.

The drive sends various status signals, read data, read clock, and servo clock information to the controller. These signals are used by the controller to monitor and control operations performed by the drive.

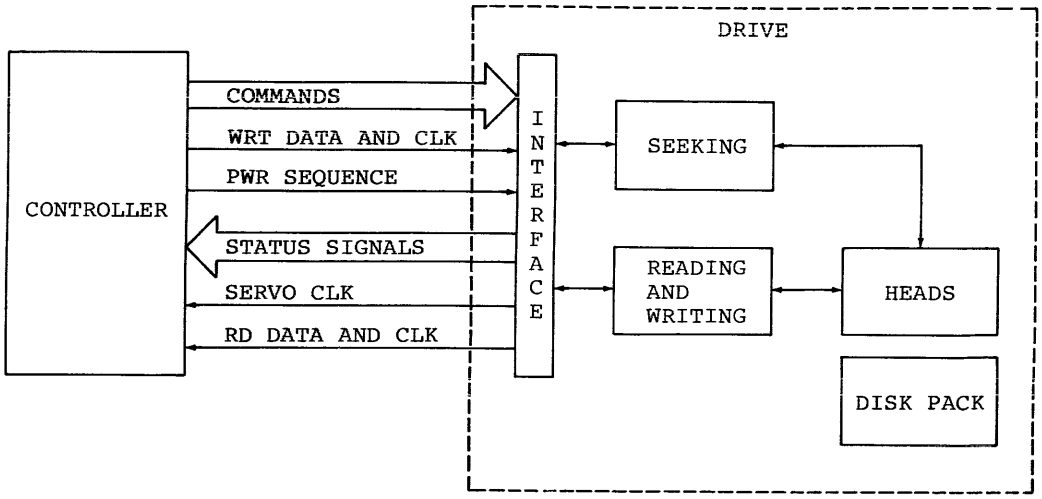


Figure 1-1. Drive Functional Blocks

SEEKING

The drive must position the heads over the desired data record before it writes or reads data. This function is called seeking and it is performed by a servo system consisting of control logic and a head positioning mechanism.

READING AND WRITING

The drive is capable of both writing data on and reading it from the disk pack. During a write operation, the drive receives data from the controller, processes it and writes it on the disk pack. During a read operation, the drive recovers data from the disk pack, and transmits it to the controller.

DRIVE PHYSICAL DESCRIPTION

GENERAL

The following describes the physical characteristics of the drive. The discussion is divided into two major areas (1) assemblies and (2) logic and circuitry.

ASSEMBLIES

The major drive assemblies are shown on figure 1-2 and described in table 1-2. A more complete description of the drive assemblies is found in the Parts Data section of the maintenance manual.

LOGIC AND CIRCUITRY

The drive contains integrated and discrete component circuits as well as relays, switches and other electromechanical elements. All of these work together in performing the various drive functions.

Diagrams showing all circuits and interconnecting wiring are contained in the maintenance manual. Sections 5 and 6 of this manual describe characteristics of individual discrete and integrated circuits.

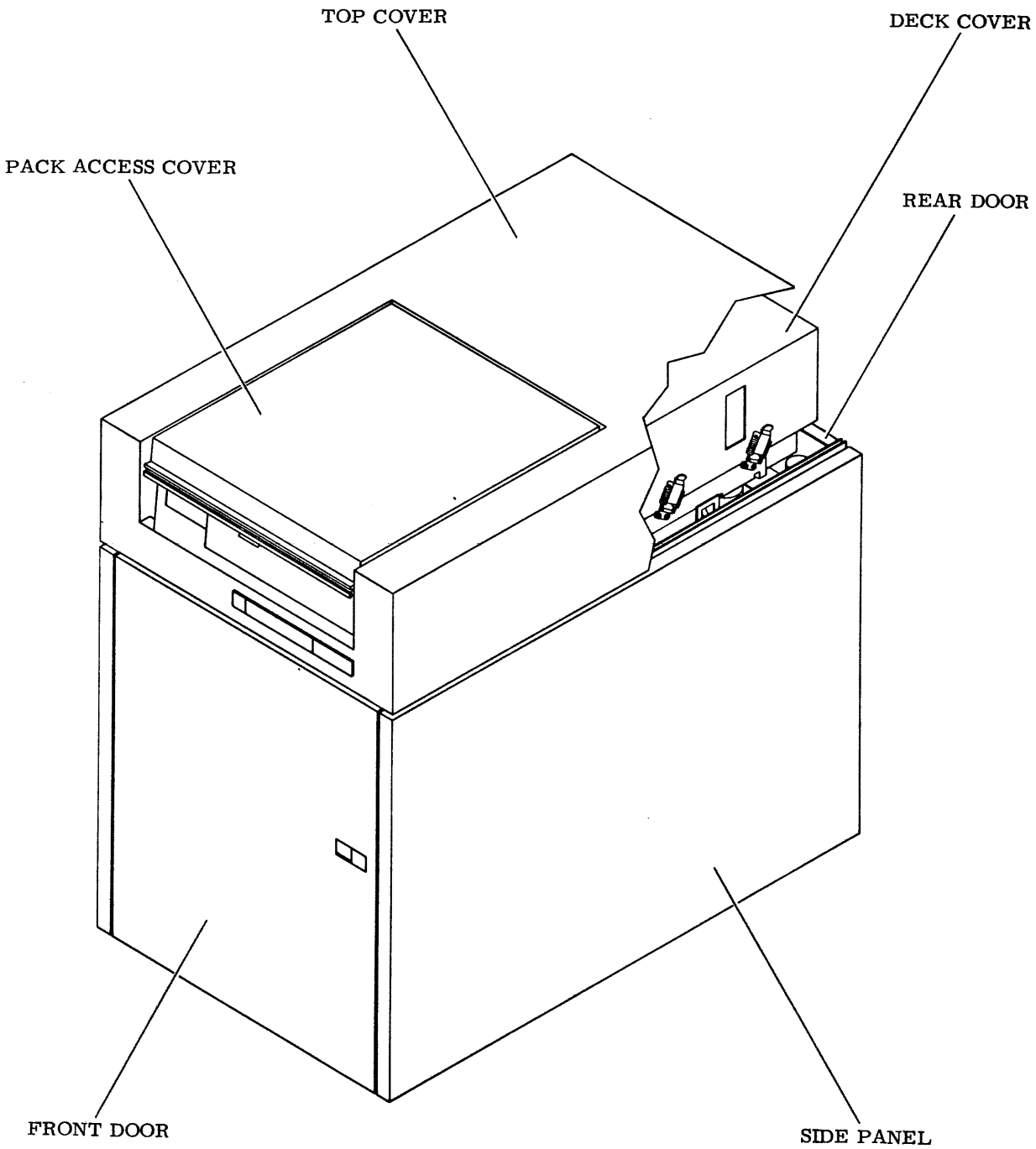


Figure 1-2. Drive Assemblies (Sheet 1 of 2)

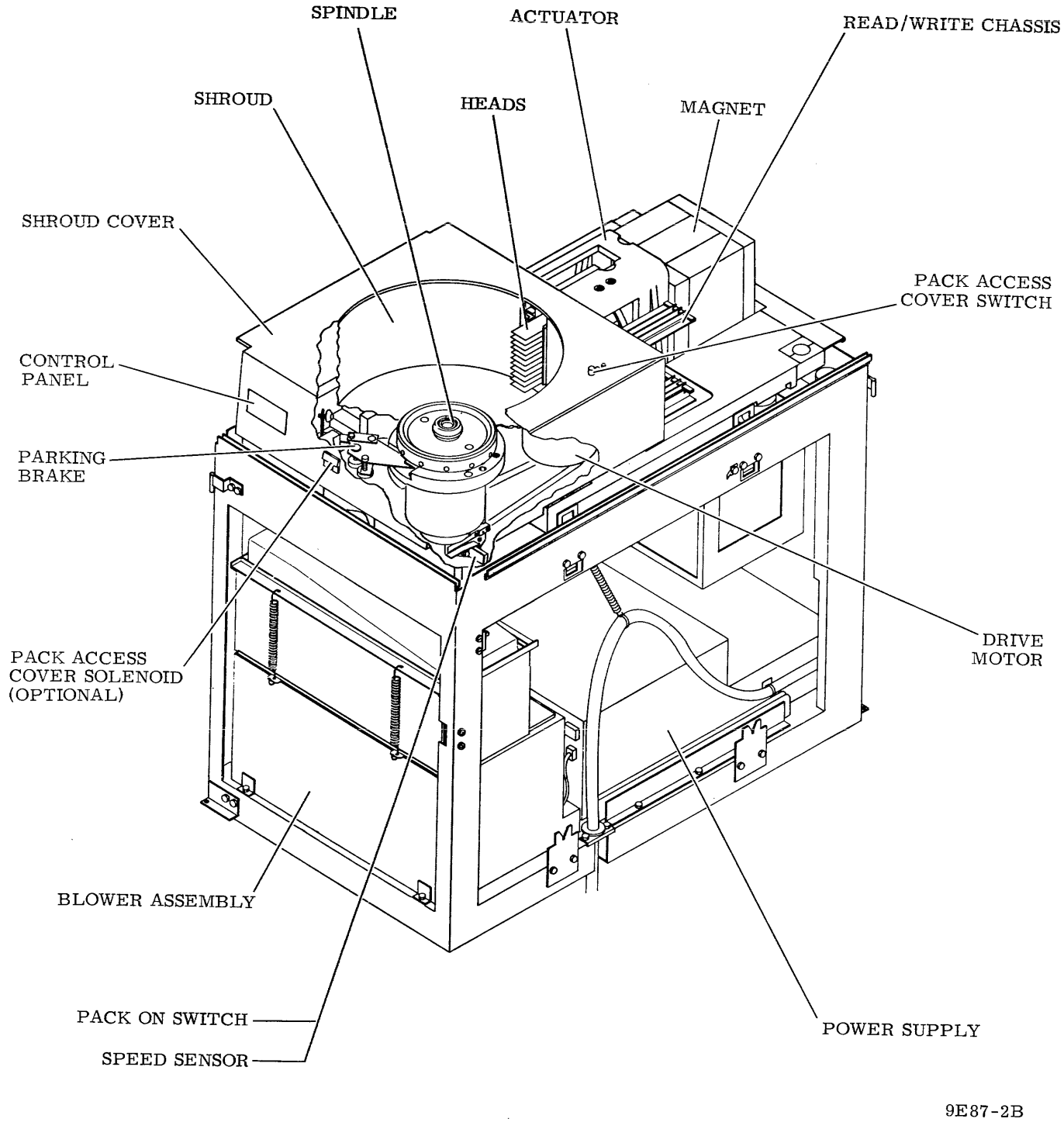


Figure 1-2. Drive Assemblies (Sheet 2 of 2)

TABLE 1-2. DRIVE ASSEMBLIES

Actuator	Contains voice coil and carriage. This assembly positions the heads over the disk pack.
Blower Assembly	Contains a blower motor that circulates cooling air for the drive.
Deck Cover	Provides an electrical interference shield for the drive and also reduces noise level output from drive.
Drive Motor	Provides rotational motion that turns spindle and disk pack.
Front Door	Provides access to blower assembly and the lower front part of cabinet.
Heads	Detect data transitions that are on the pack if drive is reading. Writes data transitions on the disk pack if drive is writing.
Logic Chassis	Contains logic cards that control operation of drive.
Magnet	Provides permanent magnetic field that is used in conjunction with voice coil to move carriage and heads.
Operator Control Panel	Contains switches that allow operator to control and monitor basic operation of drive.
Pack Access Cover	Provides access to disk pack and pack area.
Pack Access Cover Solenoid (Optional)	Prevents pack access cover from being opened if the pack is spinning.
Pack Access Cover Switch	Interlock that de-energizes drive motor if pack access cover is opened while pack is spinning. It also prevents motor from starting unless cover is closed.
Pack On Switch	Interlock that prevents drive motor from starting when pack is not installed.
Parking Brake	Holds spindle while disk pack is being installed and removed.
Power Supply	Furnishes all necessary voltages for drive operation.
Read/Write Chassis	Contains cards that are essential to drive read/write operations.
Rear Door	Provides access to power supply, logic chassis and lower rear of cabinet.
Shroud and Shroud Cover	Provides protection and ventiliation for disk pack.
Side Panels	Provide access to either side of drive.
Spindle and Lockshaft	Provides mounting surface for disk pack. Lockshaft secures disk pack to spindle. Drive motor transmits rotational motion to spindle via drive belt thereby causing disk pack to rotate.
Top Cover	Covers entire top of drive thereby protecting drive assemblies and reducing output noise level.

EQUIPMENT CONFIGURATION

GENERAL

The equipment configuration is identified by the equipment identification plate and by the FCO log. It is necessary to identify the equipment configuration to determine if the manuals being used are applicable to the equipment. The following describes the cabinet identification plate, FCO log and manual to equipment correlation.

EQUIPMENT IDENTIFICATION PLATE

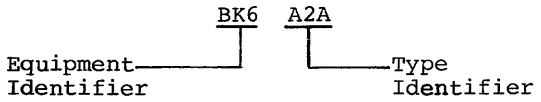
General

This plate is attached to the frame at the rear of the drive (refer to figure 1-3). This plate identifies the drives basic mechanical and logical configuration at the time it leaves the factory. The information contained on this plate is defined in the following.

Equipment Identification Number

This number is divided into the two parts shown in the example:

EXAMPLE:



The equipment identifier indicates the basic functional capabilities of the drive. This number will be either BK6 or BK7. The differences between these units can be determined by referring to table 1-1.

The type identifier indicates differences between drives that have the same equipment number. These differences are necessary to adapt a drive to specific system requirements. However, they do not change the overall capabilities of the drive as defined in table 1-1.

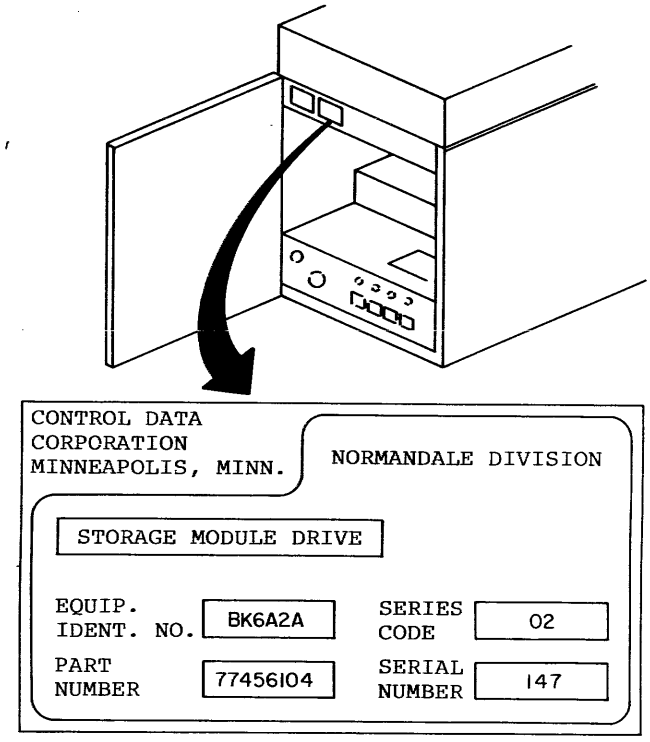


Figure 1-3. Equipment Identification Plate

The various types differ according to their input voltage requirements and standard options. The standard options are those features with which the drive is equipped when it leaves the factory. The Configuration Chart in the front matter of this manual lists both input voltage requirements and standard options for all types of BK6 and BK7 drives.

The standard options listed in this chart are as follows:

- A Cable I/O - Drive A cable connector may have 50, 60, or 75 pins (refer to discussion on Interface in section 3 of this manual).
- Dual Channel - Allows drive to connect to two controllers (refer to discussion on Unit Selection in section 3 of this manual).
- Index and Sector Configuration - These signals maybe carried on the A cable, B cable, or both cables.
- Pack Access Cover Solenoid - Solenoid that locks the pack access cover in the closed position when the pack is spining.
- Color Code - The color code is used in conjunction with the color code chart (table 5-1 in the hardware maintenance manual). See the introduction to Section 5 of that manual for further explanation.

Series Code

The series code represents a time period within which a unit is built. While all units are interchangeable at the system level, regardless of series code, parts differences may exist within units built in different series codes. When a parts difference exists, that difference is noted in the parts data section of the hardware maintenance manual.

Part Number

This number indicates the top level assembly number of the equipment and is for factory use only.

Serial Number

Each drive has a unique serial number assigned to it. Serial numbers are sequentially within a family of drives. Therefore, no two equipments will have the same serial number.

FCO LOG

Field Change Orders (FCO's) are electrical or mechanical changes that may be performed either at the factory or in the field. FCO changes do not affect the series code but are indicated by an entry on the FCO log that accompanies each machine. The components of a machine with an FCO installed may not be interchangeable with those of a machine without the FCO; therefore, it is important that the FCO log be kept current by the person installing each FCO.

MANUAL TO EQUIPMENT CORRELATION

Throughout the life cycle of a machine, changes are made either in the factory build (a series code change) or by FCOs installed in the field. All of these changes are also reflected in changes to the manual package. In order to assure that the manual correlates with the machine, refer to the Manual To Equipment Correlation sheet located in the front matter of the hardware maintenance manual. This sheet records all the FCOs which are reflected in the manual. It should correlate with the machine FCL log if all the FCOs have also been installed in the machine.

SECTION 2

OPERATION

OPERATION 2

INTRODUCTION

This section provides the information and instructions necessary for operating the drive and is divided into the following areas:

- Controls and Indicators - Locates and describes various controls and indicators related to operation of the drive.
- Operating Instructions - Describes procedures for operating the drive.

CONTROLS AND INDICATORS

GENERAL

The drive has two basic types of operator controls and indicators. These are (1) Operator control panel (2) power supply control panel. These are shown on figure 2-1 and explained in the following.

NOTE

Additional controls and indicators contained on cards in the Logic Chassis and used primarily for maintenance are described in the hardware maintenance manual.

OPERATOR CONTROL PANEL

The operator control panel contains switches and indicators to control and monitor the basic operation of the drive. Figure 2-1 shows these controls and indicators and table 2-1 explains their functions.

POWER SUPPLY CONTROL PANEL

The power supply control panel contains circuit breakers, test points and a time meter. These provide the means of controlling and monitoring operation of the power supply. The control panel is accessed by opening the rear door of the drive cabinet. Figure 2-1 shows the power supply control panel and table 2-2 explains their functions.

OPERATING INSTRUCTIONS

GENERAL

This discussion describes the procedures that are performed during normal operation of the drive. These procedures are: disk pack storage, disk pack removal and installation, power on and off.

DISK PACK STORAGE

To ensure maximum disk pack life and reliability, observe the following precautions:

- Store disk packs in machine-room atmosphere ($60^{o}F$ to $90^{o}F$, 10% to 80% relative humidity).
- If disk pack must be stored in different environment, allow two hours for adjustment to computer environment before use.
- Never store disk pack in direct sunlight or in dirty environment.
- Store disk packs flat, not on edge. They may be stacked with similar packs when stored.
- Always be sure that both top and bottom plastic covers are on disk pack and locked together whenever it is not actually installed in a drive.
- When marking packs, use pen or felt tip marker that does not produce loose residue. Never use a lead pencil.
- Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack cannister if required.
- Cleaning of pack surfaces is not recommended.

DISK PACK HANDLING (CE AND DATA PACKS)

The positive pressure filtration system of the drive eliminates the need for periodic inspection and cleaning of the disk pack (media). However, should improper operating conditions of the pack be indicated by any of the following symptoms, immediately remove the pack from the drive.

1. A sudden increase in error rates related to one or more heads is observed.
2. An unusual noise such as pinging or scratching is heard.
3. A burning odor is smelled.
4. Contamination of the pack from dust, smoke, oil or the like is suspected.

If any doubt about the pack's functional condition exists, return it to the vendor, enclosing a description of the known or suspected malfunction.

CAUTION

Do not attempt to operate the media on another drive until full assurance is made that no damage or contamination has occurred to the media.

Do not attempt to operate the drive with another media until full assurance is made that no damage or contamination has occurred to the drive heads or to the shroud area.

DISK PACK INSPECTION AND CLEANING

In some cases, the user may attempt to inspect and clean the disk pack rather than return it to the vendor. This task must be performed by properly trained personnel only, using the following procedure.

NOTE

Inspection and cleaning of disk packs in the field can cause additional problems for the following reasons:

- Exposure of the pack to non-cleanroom conditions during inspection and cleaning may additionally contaminate the pack.
- Disk surfaces may be scratched by using contaminated or improper cleaning equipment.
- The pack may be damaged while the covers are removed.
- Deposits of cleaning solution residue may be left on disk surface if improperly cleaned or if commercial grade solutions are used.

CAUTION

Disk pack cleaning should never be attempted with the pack mounted on the drive, since this setup can introduce contamination into the drive itself.

1. Mount the pack on a commercially available pack inspection fixture.
2. Dampen, but do not soak, a lint-free swab-paddle with media cleaning solution (refer to the list of Maintenance Tools and Materials), or with a solution of 91% reagent grade isopropyl alcohol and 9% deionized water by volume.
3. Using a sweeping motion, insert the damp swab-paddle between the disks and manually rotate the pack while applying the swab-paddle lightly to the disk surface to be cleaned.
4. After the swab-paddle has been applied for one full cleaning rotation, withdraw it with a sweeping motion while maintaining contact with the disk surface (do not lift the swab-paddle from the surface).
5. If oxide or contaminants are observed on the swab-paddle, repeat steps 2, 3, and 4, using a clean swab-paddle for each pass, until no oxide or contaminants are observed on the swab-paddle.
6. Repeat steps 3 and 4 using a dry swab-paddle to remove all cleaning solution residue.
7. Repeat steps 2 through 6 for each surface.

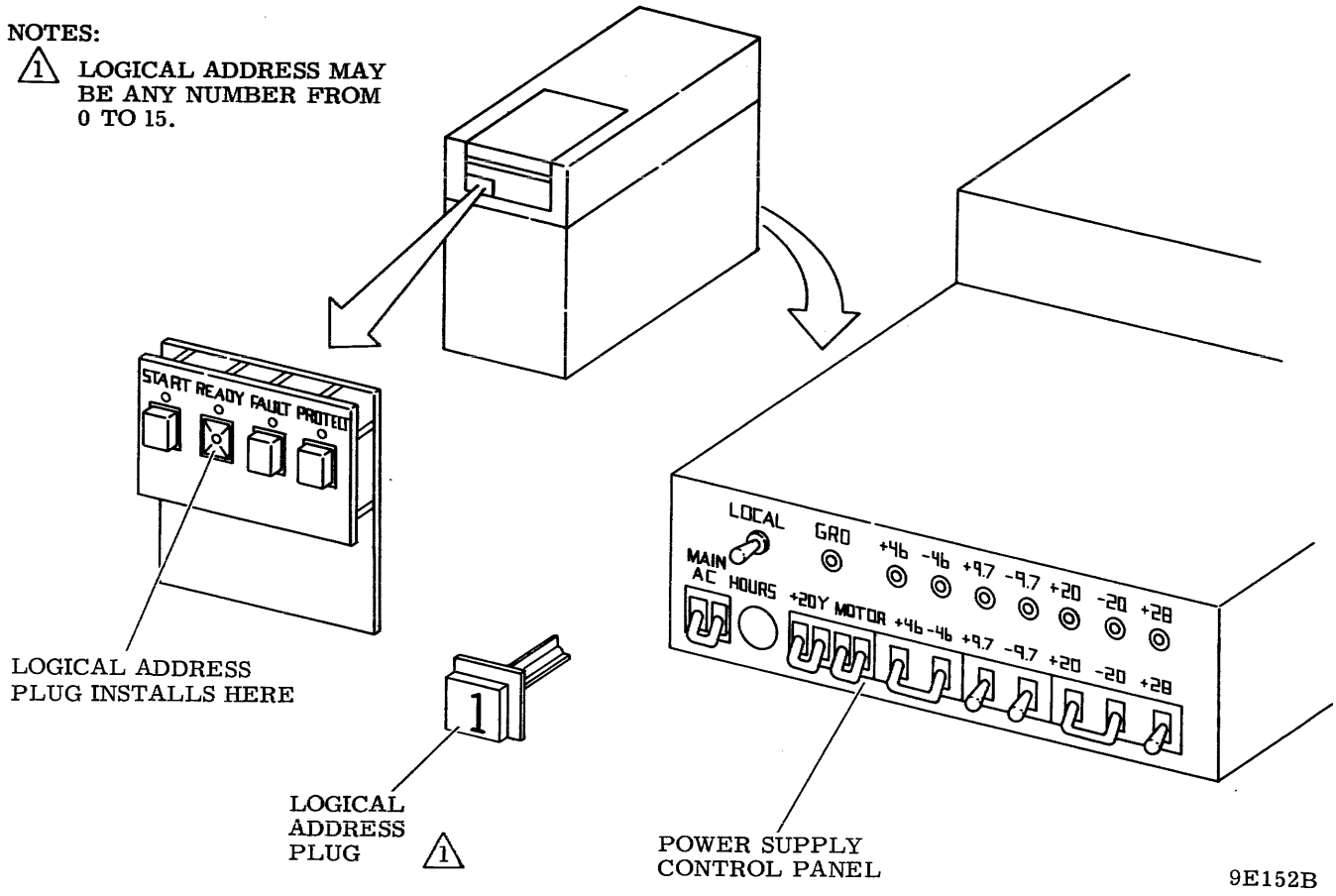


Figure 2-1. Controls and Indicators

TABLE 2-1. OPERATOR CONTROL PANEL FUNCTIONS

Control or Indicator	Function
Logical Address Plug	Determine logical address of drive. Address can be set any number from 0 to 15 by installing the proper plug. If no plug is installed the address is 15. Drive comes from the factory with complete set of logical address plugs each having a unique address. The available plugs with their associated address and part number are listed in the parts data section of the hardware maintenance manual.
START Switch/ Indicator	Pressing button when drive is in power off condition (disk pack not spinning) lights indicator and starts power on sequence, provided the following conditions are met. • Disk pack is installed. • Pack access cover is closed. • All power supply circuit breakers are on. Pressing the indicator when drive is in power on condition (disk pack spinning), extinguishes indicator and starts power off sequence.
READY Indicator	Lights when unit is up to speed, the heads are loaded and no fault condition exists.
FAULT Switch/Indicator	Lights if a fault condition exists within the drive. It is extinguished by any of the following providing reason for fault is no longer present: • Pressing FAULT switch on operator control panel • Fault Clear signal from controller • Maintenance Fault Clear switch on fault card in logic chassis location A17. Conditions causing fault are described in the discussion on Fault Detection in section 3 of this manual.
WRITE PROTECT Switch/Indicator	Pressing switch to light indicator disables the driver write circuits and prevents it from writing data on the pack. Pressing the switch to extinguish the indicator removes the disable from the write circuits.

TABLE 2-2. POWER SUPPLY CONTROL PANEL FUNCTIONS

Control or Indicator	Function
MAIN AC Circuit breaker	Controls application of site AC power to drive. Closing this breaker applies power elapsed time meter.
HOURS Elapsed time meter	Records accumulated AC power on time. Meter starts when MAIN AC circuit breaker is closed.
LOCAL/REMOTE Switch	Controls whether drive can be powered up from drive (LOCAL) or controller (REMOTE). In LOCAL position, drive power on sequence starts when START switch is pressed. In REMOTE position, drive power on sequence starts when START switch is pressed and sequence power ground is received from controller.

Table continued on next page

TABLE 2-2. POWER SUPPLY CONTROL PANEL FUNCTIONS (Contd)

Control or Indicator	Function
+20Y, MOTOR, +46, -46, +9.7, -9.7, +20, -20, +28	Controls application of associated voltages to drive and also provides overload protection.

DISK PACK INSTALLATION

The disk pack must be installed prior to performing any drive operations. Disk Pack installation consists of setting the pack on the drive spindle and rotating the pack until the pack lockscrew is locked to the spindle lockshaft. The following describes this procedure.

CAUTION

Make certain that no dust or other foreign particles are present in shroud area. Also, ensure that blowers operate for at least two minutes prior to disk pack installation in order to purge blower system.

1. Set circuit breakers to on and observe that blower starts.
2. Raise pack access cover.
3. Disengage bottom dust cover from disk pack by squeezing levers of release mechanism in center of bottom dust cover and set cover aside to an uncontaminated storage area.

CAUTION

Non-fully retracted heads indicate a problem in the drives servo, and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

NOTE

Top dust cover actuates parking brake when pack is set on spindle. Actuating brake holds spindle stationary while pack is installed. A click is heard as brake engages.

4. Set disk pack on spindle, avoiding abusive contact between disk pack and spindle, then twist clockwise until it is secured to spindle lockshaft.
5. Lift top dust cover clear of drive and store it with bottom dust cover.

CAUTION

Spin pack to ensure that removing top dust cover released parking brake.

6. Close pack access cover immediately to prevent entry of dust and contamination of disk surfaces.

DISK PACK REMOVAL

Disk pack removal consists of removing the pack from the spindle, installing the dust covers and setting the pack aside in an uncontaminated storage area. The following describes this procedure.

1. Press START switch to stop drive motor and unload heads.
2. When disk pack rotation has stopped completely, open pack access cover.

CAUTION

Non-fully retracted heads indicate a problem in the drives servo, and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

3. Place top dust cover over disk pack so post protruding from center of disk pack is received into dust cover handle.
4. Turn cover counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between disk pack and spindle.

5. Lift top cover and disk pack clear of drive and close pack access cover.
6. Place bottom dust cover on disk pack and store pack in an uncontaminated storage area.

POWER ON PROCEDURE

The following procedure describes how power is applied to the drive.

1. Set all power supply circuit breakers to on, and observe that blowers start.

CAUTION

Allow blowers to operate for at least two minutes before installing disk pack.

2. Install disk pack as instructed in disk pack installation procedure.

3. Set LOCAL/REMOTE switch to desired position.

4. Press START switch to light START indicator. If drive is in Local mode, drive motor starts immediately and heads will load when motor is up to speed. If drive is in remote mode, drive motor starts and heads load whenever sequence power ground is available from controller (refer to discussion on power system in section 3 of this manual).

5. Observe that READY indicator lights when heads have loaded. The drive is now ready for online operations.

POWER OFF PROCEDURE

The power off sequence can be started either locally or remotely depending on the setting of the LOCAL/REMOTE switch. If this switch is in LOCAL, the sequence starts when the START switch is pressed to extinguish the START indicator. If the switch is in REMOTE, the sequence starts either when the START switch is pressed or when the sequence power ground signal is disabled at the controller (refer to discussion on Power System in section 3 of this manual).

In either case, the power off sequence unloads the heads, stope the drive motor and extinguishes the READY indicator.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 3-1):

- Power System Functions - Describes how the drive provides the voltage necessary for drive operation.
- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drives disk pack rotation, head positioning and air flow systems.
- Interface Functions - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.
- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.
- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disk pack.
- Machine Clock Functions - Explains how this circuit uses signals derived from the disk pack to generate timing pulses for the index, sector and read/write circuits.
- Index Detection - Describes how the drive detects the index pattern which is used to indicate the logical beginning of each track.
- Sector Detection - Explains how the drive derives the sector pulses, which are used to determine the angular position, with respect to Index of the read/write heads.
- Head Selection - Explains the head selection process.

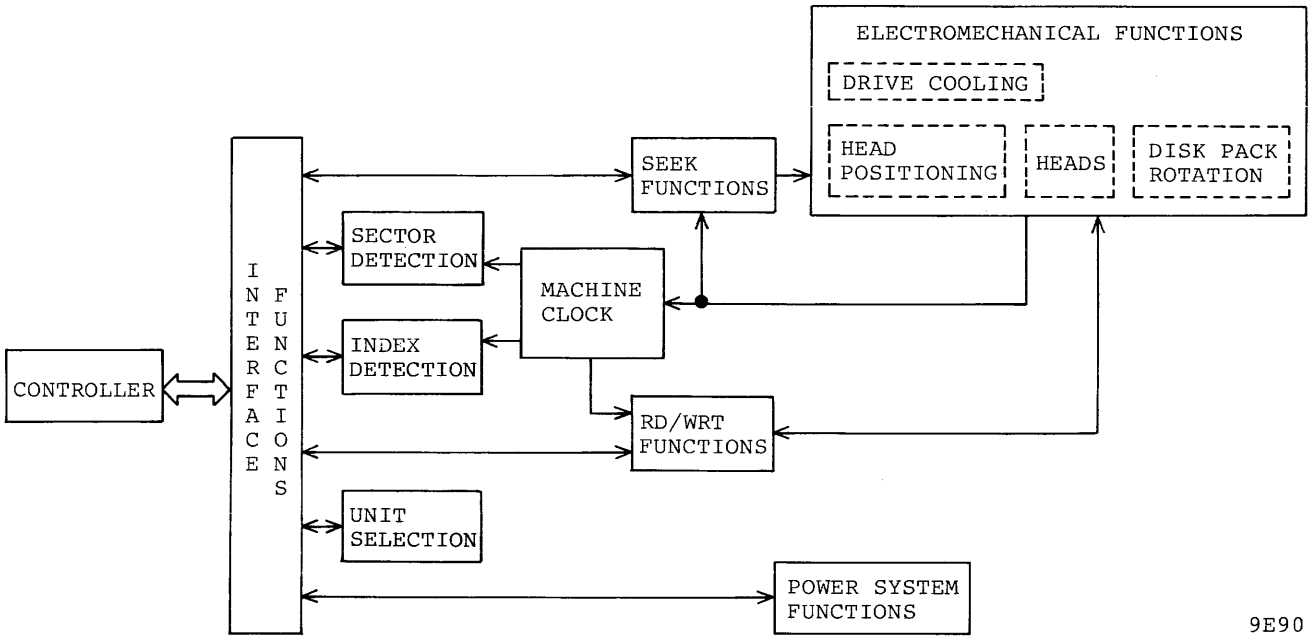


Figure 3-1. Drive Functional Block Diagram

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk pack.

- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in the hardware maintenance manual should take precedence over those in this manual if there is a conflict between the two.

POWER SYSTEM FUNCTIONS

GENERAL

The major element in the drives power system is the power supply. The power supply receives its input from the site ac power source and uses it to produce all the ac and dc voltages necessary for drive operation. These voltages are distributed to the drive circuitry via circuit breakers.

The drive motor is started and heads load function initiated during the power on sequence. The power off sequence unloads the heads and stops the drive motor. The drives LOCAL/REMOTE switch permits these sequences to be initiated either at the drive (local) or at the controller (remote).

The remainder of this discussion provides further description of the power system and is divided into the following areas:

- Power Distribution - Describes how the power is distributed to the drive circuitry.

- Local/Remote Power Sequencing - Explains how the drive may be powered up either at the drive or the controller.

- Power On Sequence - Describes how power is applied to the drive motor and the heads load sequence initiated.

- Power Off Sequence - Describes how the heads are unloaded and the drive motor stopped.

- Emergency Retract - Explains sequence performed when conditions exist requiring the heads be unloaded immediately to avoid damage to them or the disk pack.

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power supply and rest of the drive so that the power on sequence can be performed. The distribution is controlled by circuit breakers located within the power supply. These circuit breakers also provide overload protection for their associated voltages. The power distribution circuits are shown on figure 3-2 and basic operation is explained in the following.

Site main ac power is input to the power supply via the MAIN AC circuit breaker. When this breaker is closed, it applies power to the HOUR meter. It also providess the input to the drive motor control triacs; however, the motor does not start until the power on sequence.

Closing CB2 applies power to T3 and enables +20Y. With +20Y available, the transformers control triacs are enabled and power is applied to transformers T1 and T2 and the blower motor. These transformers provide inputs to the rectifier and capacitor board (-YEN), which in turn produces the dc voltages. The dc voltages are applied to the rest of the drive when their associated circuit breakers are closed.

When all circuit breakers are closed, the drives power on sequence can begin.

LOCAL/REMOTE POWER SEQUENCING CONTROL

General

The power on and off sequence of each drive can be controlled either locally or remotely depending on the setting of its LOCAL/REMOTE switch. When this switch is set to LOCAL, the sequences are initiated at the drive. When the switch is set to REMOTE, the sequences are initiated at the controller.

The LOCAL/REMOTE switch is located on the power supply control panel and controls the mode of operation by determining how the drives sequence power relay (K1) is energized and de-energized. This relay works in conjunction with the drives START switch to control the power on and off sequences.

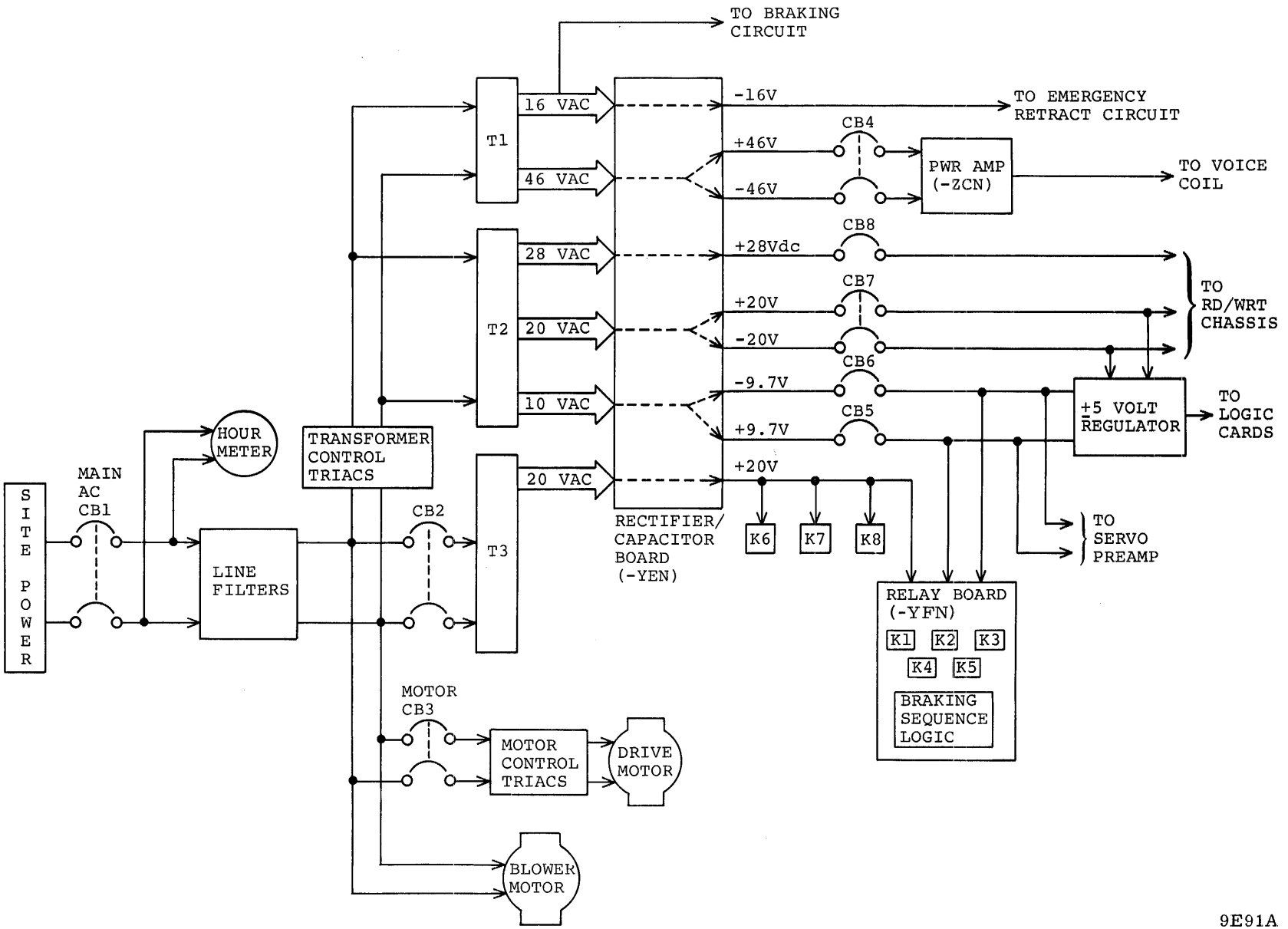


Figure 3-2. Power Distribution

Figure 3-3 shows the LOCAL/REMOTE power sequencing control circuits. The operation of these circuits in both local and remote modes is explained in the following paragraphs.

Local Control

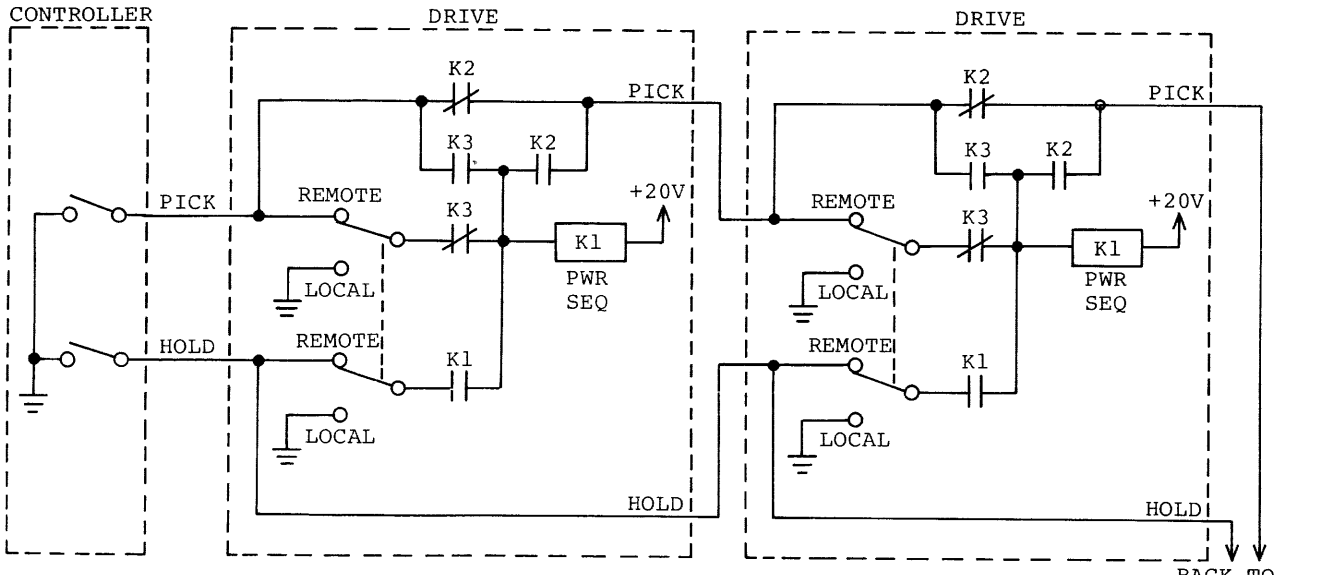
When the drive is in the local mode, the sequence power relay (K1) energizes whenever +20Y is available. This voltage is available whenever the MAIN AC circuit breaker (CB1) and +20Y circuit breaker (CB2) are closed. In this mode, the power on sequence begins when the START switch is pressed (providing all circuit breakers are closed). **The power off sequence** is initiated by pressing the START switch to extinguish the indicator. Figure 3-4 is a flow chart of the local power control sequence.

Remote Control

If the drive is in remote mode, the power sequence relay (K1) is energized by the power Sequence signals (Pick and Hold) from the controller. Therefore, even if the START switch is pressed, the power on sequence does not begin until the power sequence signals go active and energize the sequence power relay.

This makes it possible to power up drives sequentially in a system where the power sequence lines are connected in a daisy chain. A sequential power up prevents the current surge that would occur if a number of drives were powered up simultaneously.

Only the drives in the remote mode with their START switches on (lighted) are involved in the power up. Those drives in local mode or with the START switches off (light extinguished) are not involved in the power up and have no effect on it.



NOTES:
1. ALL RELAYS SHOWN IN THEIR NORMAL POWER OFF CONDITION.
2. TERMINATED AT LAST DRIVE IN CHAIN.

Figure 3-3. Local/Remote Power Sequencing Control Circuits

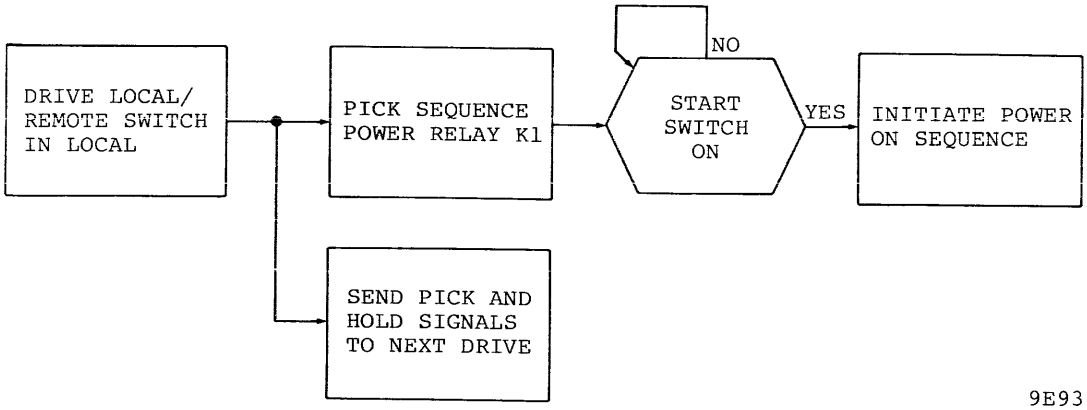


Figure 3-4. Local Mode Power Sequencing

The sequential power up occurs because each drive involved waits until its spindle is up to speed (K3 energizes) before passing the sequence signals to the next drive in the daisy chain. If a drive is not involved (local mode or START switch off) it passes the sequence signals to the next drive without delay. This continues until all drive in remote mode with START switch on are powered up. The signals are terminated at the last drive in the daisy chain.

The drives are powered down either individually by pressing the START switches, or all at once by de-activating the sequence signals at the controller.

Figure 3-5 is a flow chart of the remote power control sequence.

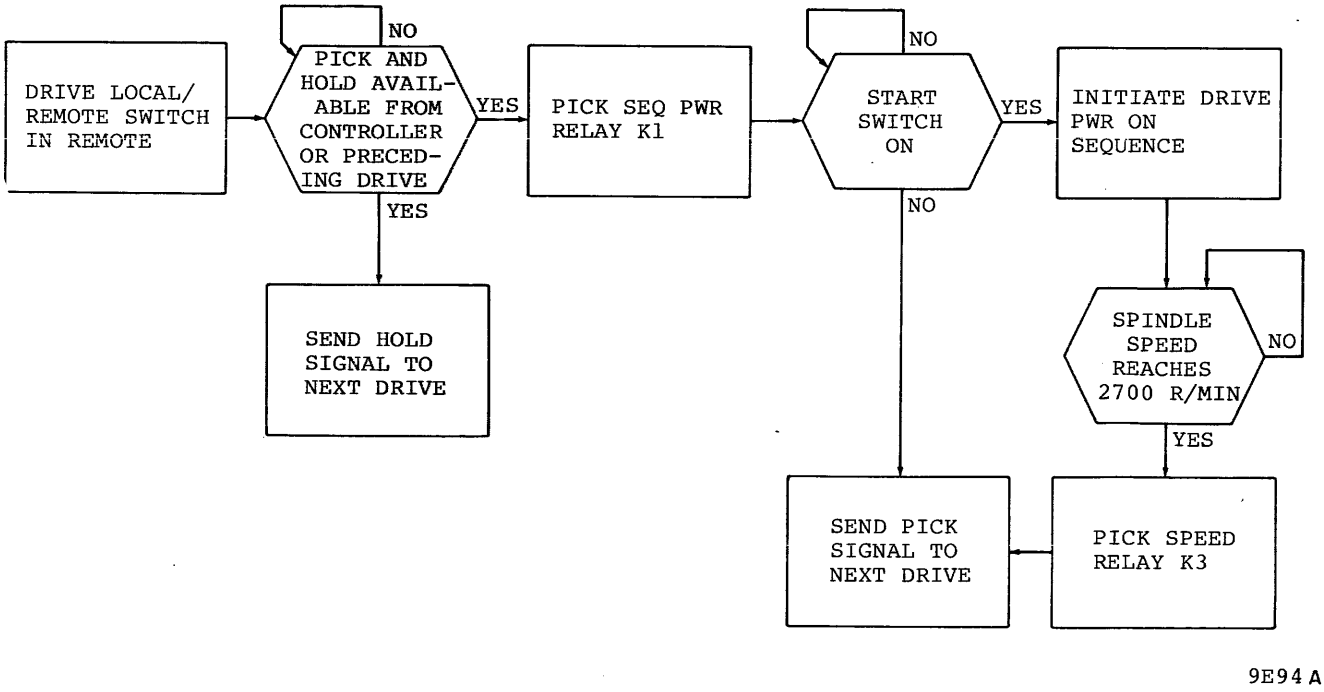


Figure 3-5. Remote Mode Power Sequencing

POWER ON SEQUENCE

The power on sequence starts the drive motor and initiates loading of the heads.

The sequence is initiated by pressing the START switch on the operator control panel. If all circuit breakers are closed, the disk pack is installed and the pack access cover is closed, pressing this switch energizes the Start relay (K2).

The Start relay causes the Motor relay (K4) to energize and enable the Motor Control triacs. This applies power to the drive motor causing it to start. The drive motor transfers motion to the spindle via the drive belt and the disk pack starts to rotate.

When the speed sensing circuits indicate the spindle speed is about 2700 r/min, the Speed relay (K3) energizes. This does two things (1) energizes the Emergency Retract relay (K7) and (2) triggers the 10 second Load Delay one shot.

Energizing the Emergency Retract relay connects the power amplifier to the voice coil and connects the Emergency Retract capacitor to -16 volts. This prepares the voice coil to respond to commands from the servo logic and charges the Emergency Retract capacitor so it is ready for an emergency retract condition.

The Heads Load Delay allows the spindle time to reach 3000 r/min before enabling the heads load logic. When the delay times out, the heads load sequence is initiated causing the heads to load. This sequence is covered in the discussion on Load Seeks.

Figure 3-6 shows the circuitry involved in the power up sequence and figure 3-7 is a flow chart of the operation.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor.

The sequence begins when either the START switch is pressed or the Sequence Power relay (K1) is de-energized. In either case the Start relay (K2) de-energizes and the RTZ logic is enabled (refer to discussion on Return to Zero Seeks). This causes the heads to move in the reverse direction.

When the heads unloaded switch indicates the heads are unloaded, the RTZ logic is disabled and the motor relay (K4) is de-energized. De-energizing the Motor relay (K4) removes power from the drive motor and enables the braking logic. Enabling the brake logic initiates the braking sequence.

The braking sequence begins by energizing the Brake Power relay (K5) which in turn energizes the Brake relay (K8). The Brake relay applies -16 Vdc across the run winding of the drive motor. The -16 Vdc causes a current to flow through the winding and the magnetic field generated by this current has a braking effect on the motor.

The motor slows down and when its speed is less than 2700 r/min, the Speed relay (K3) de-energizes. This in turn causes the Emergency Retract relay (K7) to de-energize thus disconnecting the power amplifier from the voice coil.

The Brake power and Brake relays de-energize approximately 30 seconds after the start of the braking sequence. This removes braking voltage from the drive motor, which by this time is stopped. This also removes power from the pack access solenoid thus allowing the pack access cover to be opened.

Figure 3-8 shows the circuitry involved in the power off sequence and figure 3-9 is a flow chart of the operation.

EMERGENCY RETRACT

The emergency retract function provides an emergency means of retracting the heads from the pack area. This sequence is initiated if disk speed is reduced or if conditions indicate that it may be reduced. Failure to retract the heads under these conditions could result in head crash a subsequent damage to the heads and disk pack.

Any of the following conditions initiate an emergency retract sequence:

- Loss of AC Power - If site ac power is lost, all dc power is also lost. This power loss includes +20Y, +9.7, and -16, any of which cause an emergency retract to occur.
- Loss of +20Y, -16, or +9.7 Vdc - Loosing any of these voltages directly causes the emergency retract relay to de-engerize thus starting the emergency retract sequence.
- Loss of Speed - If spindle motor speed drops below 2700 r/min, the speed detection circuits cause the emergency retract capacitor to de-energize.

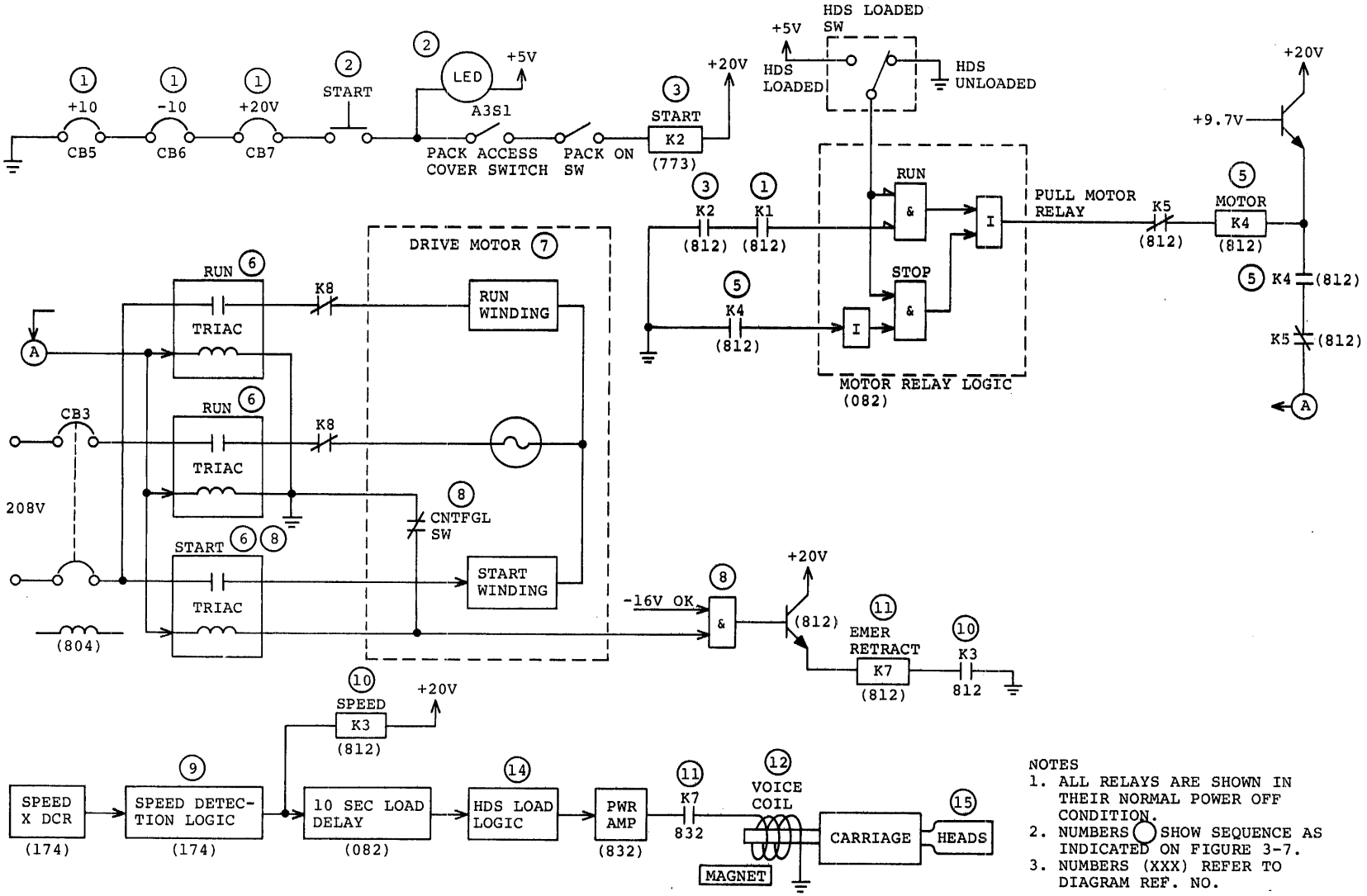


Figure 3-6. Power On Circuit

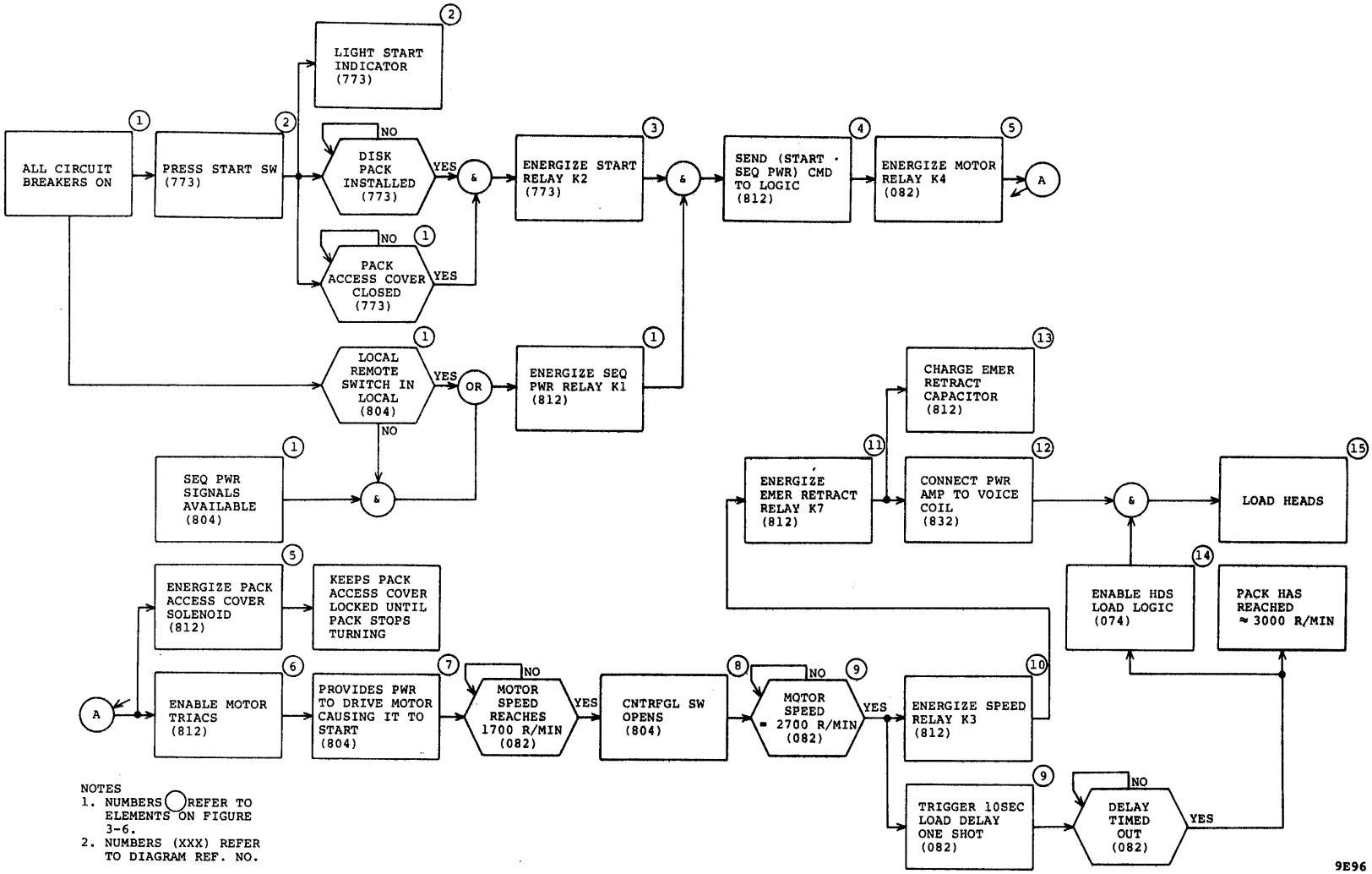


Figure 3-7. Power On Sequence Flow Chart

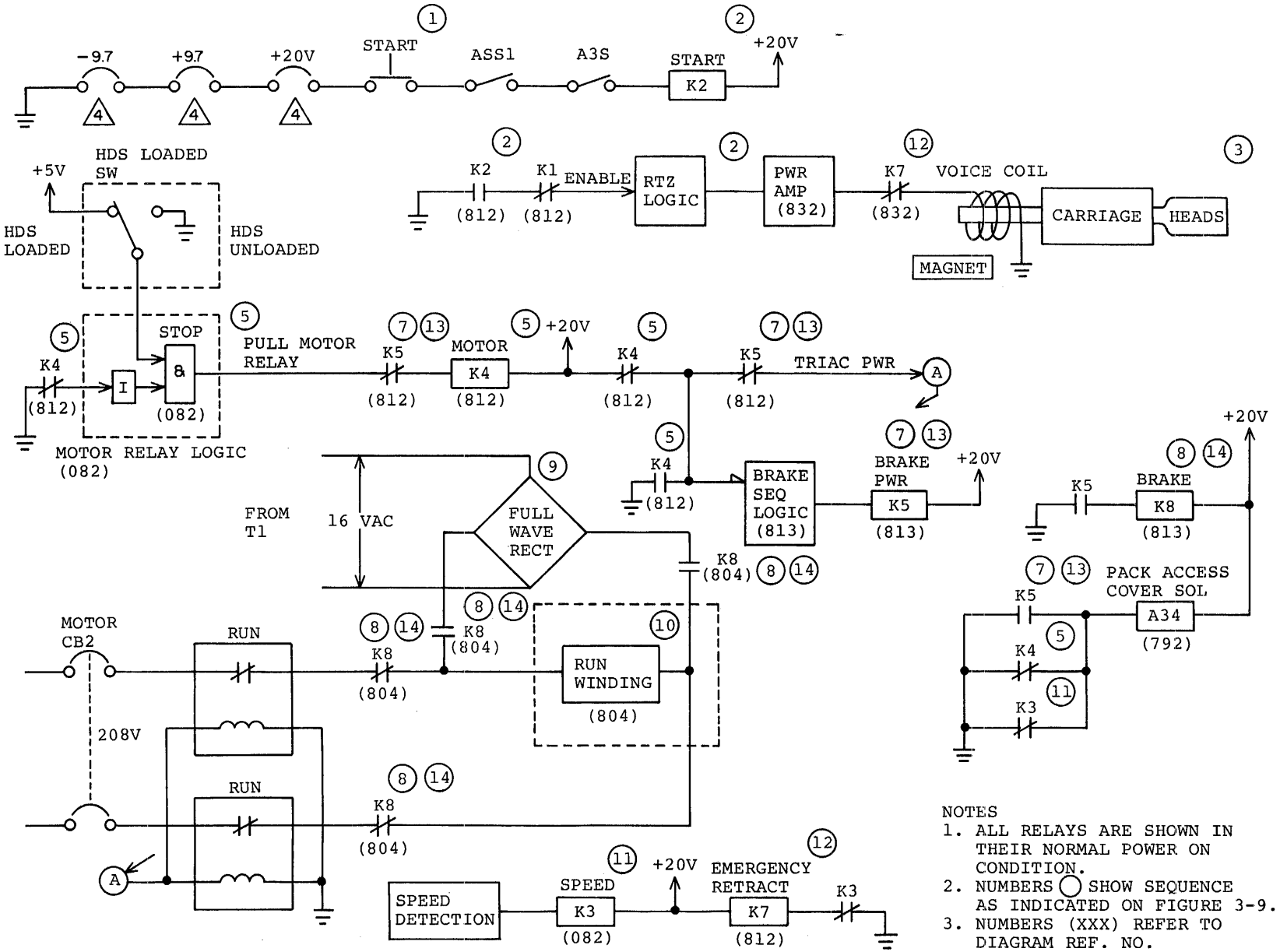


Figure 3-8. Power Off Circuits

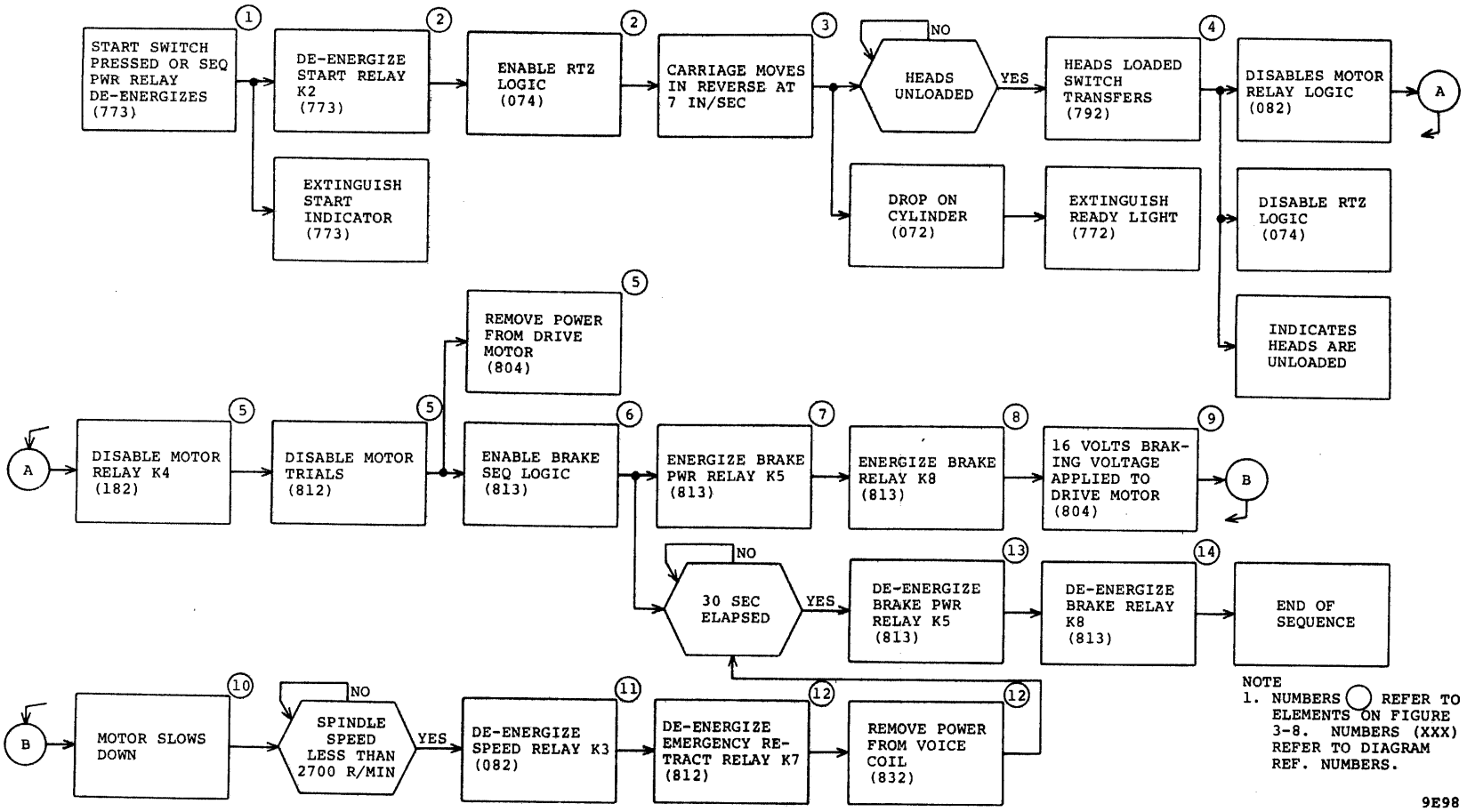


Figure 3-9. Power Off Sequence Flow Chart

- Drive Motor Thermal Overload - If the drive motor overheats, a thermal relay within the motor opens. This results in the Motor circuit breaker opening and removing power from the drive motor. The motor then slows down and the loss of speed causes an emergency retract.

Figure 3-10 shows the circuitry involved in the emergency retract sequence.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices working under the control of logical circuitry. These functions include disk pack rotation, head positioning, and drive cooling and ventilation.

Disk pack rotation is performed by the disk pack rotation mechanism, which is controlled by the power system. The purpose of disk pack rotation is to create a cushion of air on the disk surfaces. The cushion of air allows the heads (which read and write the data) to move over the disk surfaces without actually contacting them.

The heads are positioned over specific data tracks on the disk surface by the head positioning mechanism. The mechanism is controlled by the servo circuits (refer to discussion of Seek Operations) and the power system.

Drive cooling and ventilation is provided by the air flow system. The main element in this system is the blower motor which receives its power from the power system.

Figure 3-11 is a block diagram showing each of the previously discussed mechanisms. A more detailed physical and functional description of each is provided in the following discussions.

DISK PACK ROTATION

General

The disk pack must be rotating fast enough to allow the heads to fly before any drive operation can be performed. The following mechanisms work in conjunction with the power system to control disk pack rotation (refer to figure 3-12):

- Drive Motor - Provides rotating motion for the spindle and disk pack.

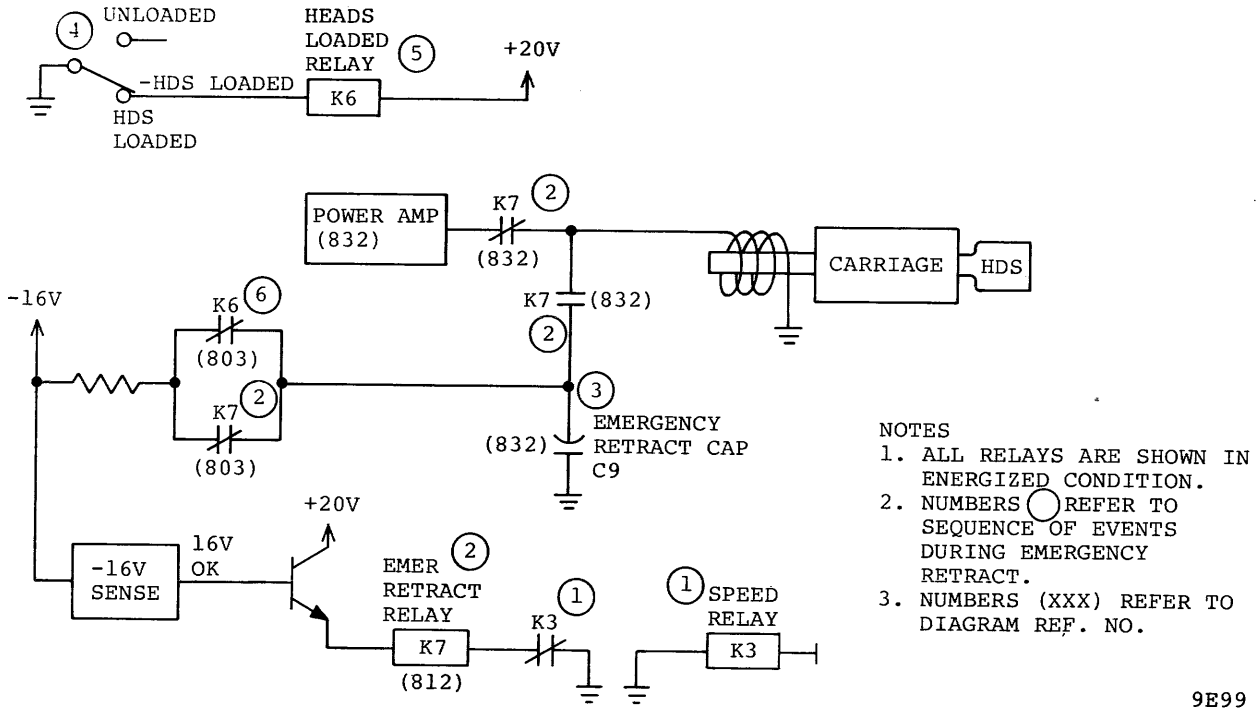


Figure 3-10. Emergency Retract Circuits

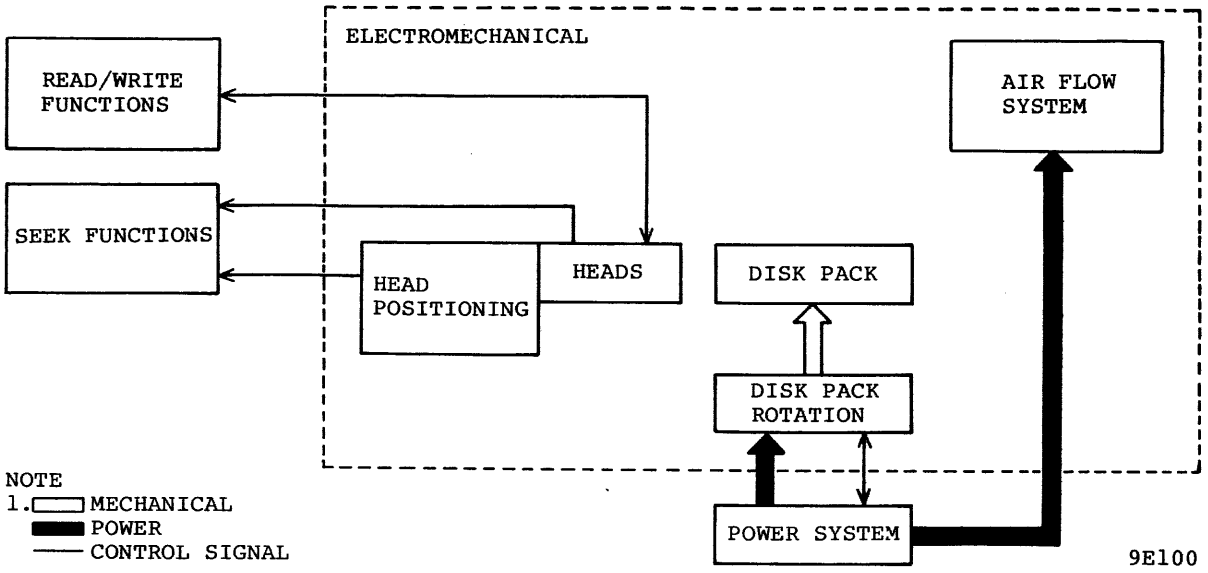


Figure 3-11. Electromechanical Functions Block Diagram

- Spindle - Provides rotating mounting surface for disk pack.
- Parking Brake - Holds spindle while pack is being installed.
- Speed Sensor - Generates pulses that are used to determine speed of spindle.
- Pack On Switch - Actuated when pack is installed on spindle, this device must indicate the pack is installed before the power on sequence can be performed.
- Pack Access Cover Switch - Ensures that pack access cover is closed before disk pack rotation begins.
- Pack Access Cover Solenoid - Prevents pack access cover from being opened while pack is rotating.

These mechanisms are further described in the following paragraphs.

Drive Motor

The drive motor provides the rotational energy required to rotate the spindle and disk pack. The motor is mounted on a movable plate which in turn is mounted on the underside of the deck casting (refer to figure 3-13).

Motion is transferred from motor to spindle via the drive belt. This belt connects the pulley on the shaft of the drive motor to the pulley on the lower end of the spindle.

The springs attached between the motor mounting plate and deck casting, maintain enough tension on the plate to keep the drive belt tight. The spring tension is adjustable so tension on the belt can be adjusted to provide the best coupling between drive motor and spindle pulleys.

The motor starts during the power on sequence when power is applied to its start and run windings (refer to Power On Sequence discussion). The start winding helps the run winding start the motor in motion and get it up to speed. When the motor speed reaches approximately 1700 r/min, the start winding is no longer needed and a centrifugal switch (within the motor) opens thus disabling the start winding. The motor continues to accelerate (using only its run winding) until it reaches it maximum speed (approximately 3600 r/min). This speed is maintained until power is removed from the motors run winding (refer to discussion on Power System).

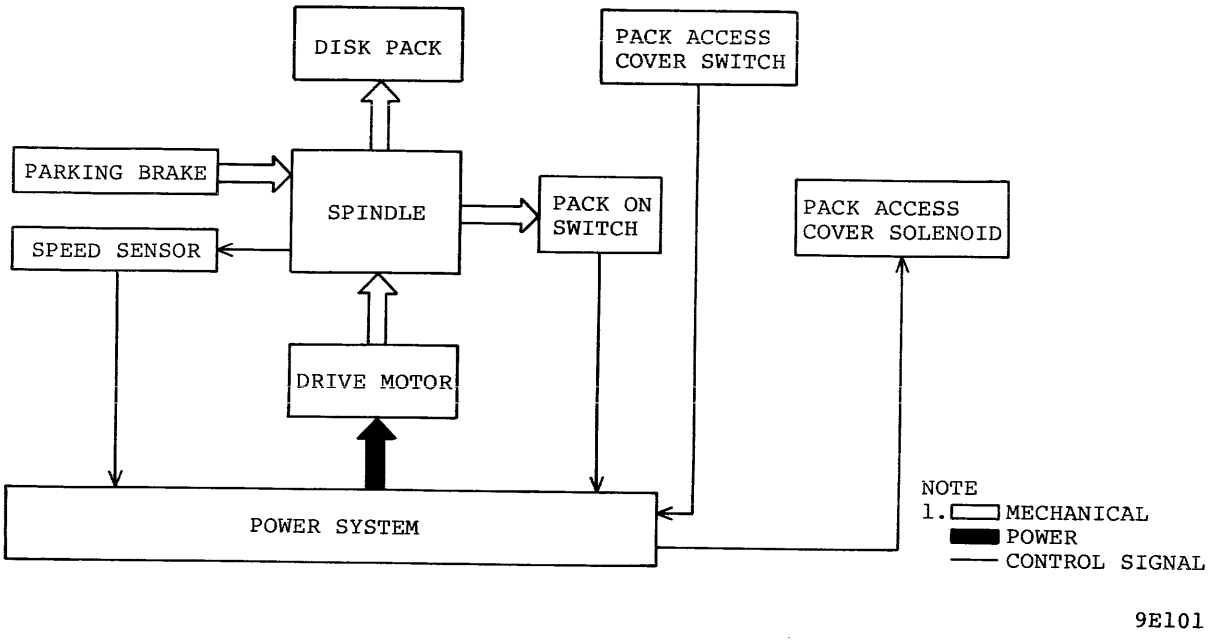


Figure 3-12. Disk Pack Rotation Functional Block Diagram

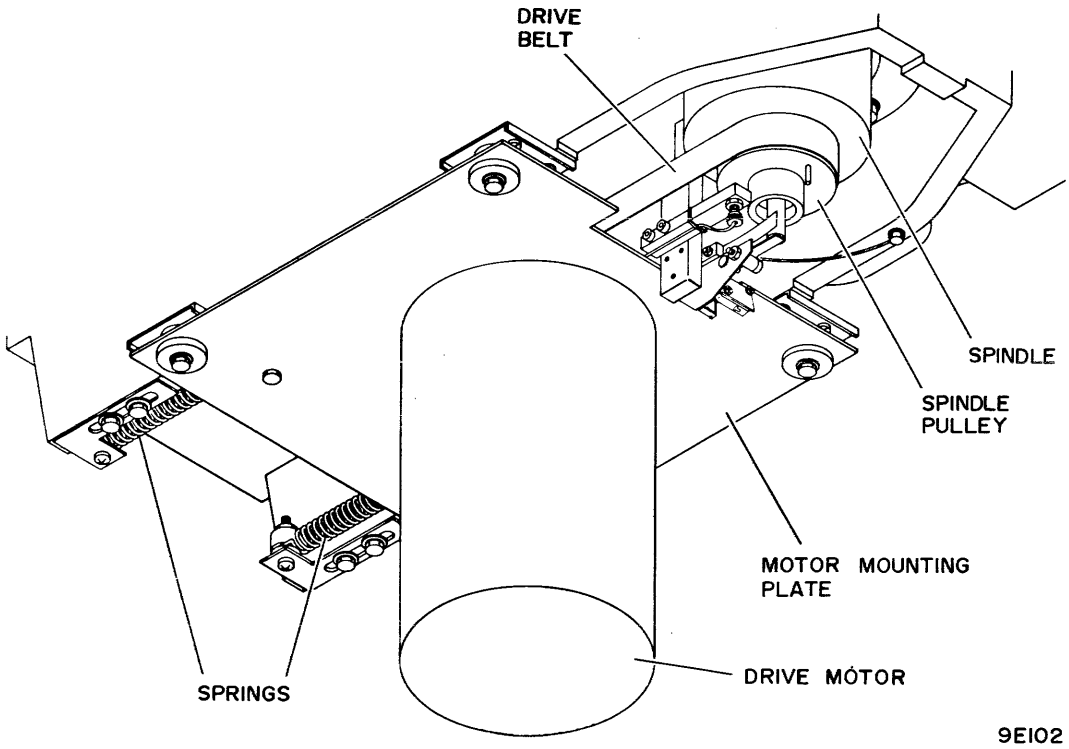


Figure 3-13. Drive Motor Assembly

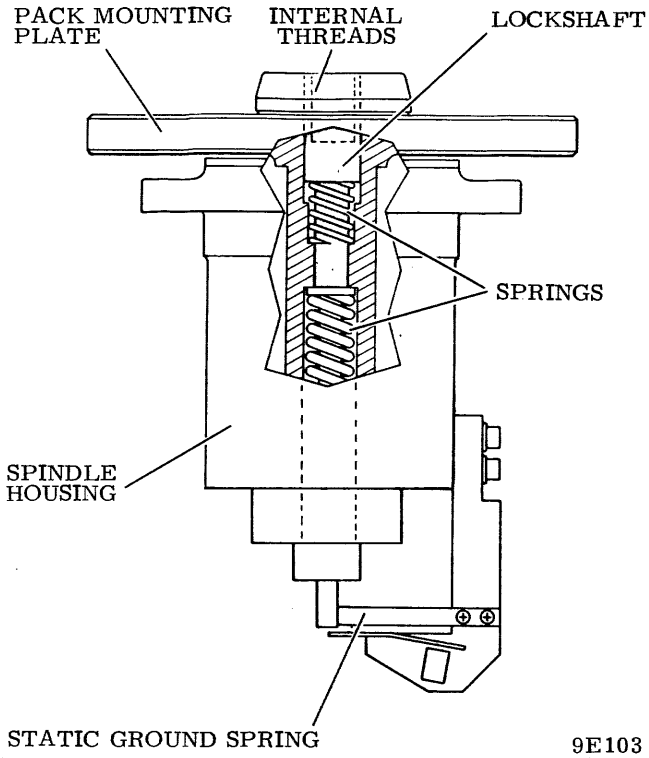


Figure 3-14. Spindle Assembly

The temperature of the motor is monitored by the thermal switch. If the motor overheats, this switch opens resulting in loss of power to the drive motor. The motor slows down causing an emergency retract and power off sequence. The drive motor cannot be restarted until it cools off, thereby causing the thermal switch to close.

Spindle

The spindle (refer to figures 3-13 and 3-14) provides the means of mounting the disk pack within the drive and also of rotating the pack when the drive motor is energized.

When the pack is mounted, its lower disk rests on the pack mounting plate. This plate connects to a shaft which in turn connects to the pulley on the lower end of the spindle. When the drive motor starts, it transfers motion to this pulley via the drive belt and causes the pack mounting plate and disk pack to rotate.

The disk pack must be secured to the mounting plate with enough force so the two of them will rotate together. This force is provided by the lockshaft, which is a spring loaded shaft located within the spindle. When the pack is installed, the mounting screw on the bottom of the pack is threaded into the internal threads in the upper end of the lockshaft. As the pack is tightened down against the mounting plate, the springs holding the lockshaft exert a downward force on the pack. When this force is sufficient, a release mechanism (in the handle of the disk pack top dust cover) releases the top dust cover from the pack. The pack is now installed and will rotate whenever the drive motor is energized.

A ground spring (refer to figure 3-13) bleeds off any static electricity accumulating on the spindle.

Parking Brake

The parking brake (refer to figure 3-15) holds the spindle stationary whenever a disk pack is installed or removed. It is actuated by the disk pack top dust cover which contacts the brake actuator button. This causes the brake tooth to move up and engage a slot in the bottom of the spindle thus preventing the spindle from rotating. When the dust cover is removed, the actuator button is released, the brake tooth disengages, and the spindle is free to turn.

Speed Sensor

The speed sensor (refer to figures 3-16 and 3-17) is a device that generates signals used to determine if spindle speed is sufficient to allow the heads to fly. The sensor is mounted beneath the spindle and consists of a small coil and core assembly. The coil has a current flowing through it and each time the pin mounted on the bottom of the rotating spindle aligns itself with the core of the coil, a signal is generated.

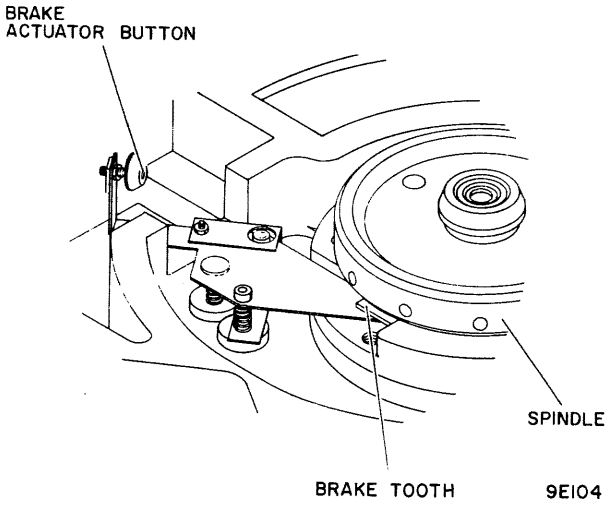


Figure 3-15. Parking Brake Assembly

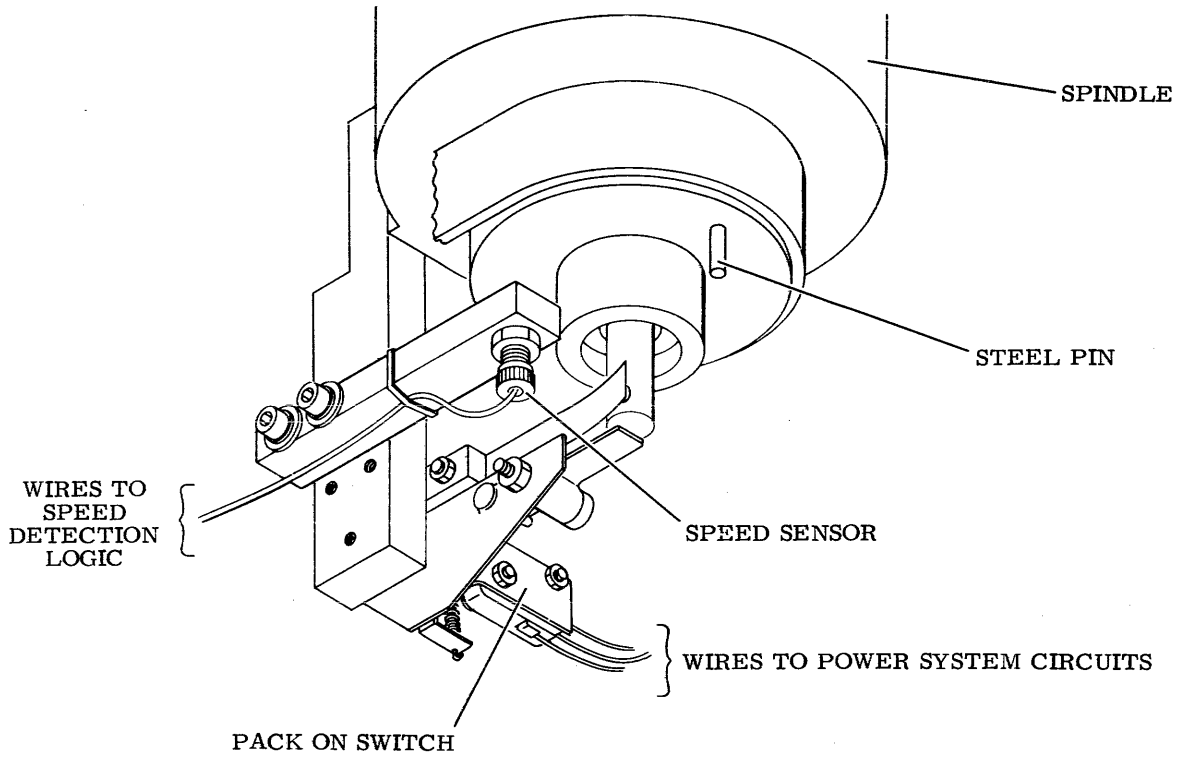


Figure 3-16. Speed Sensor and Park On Switch Assemblies

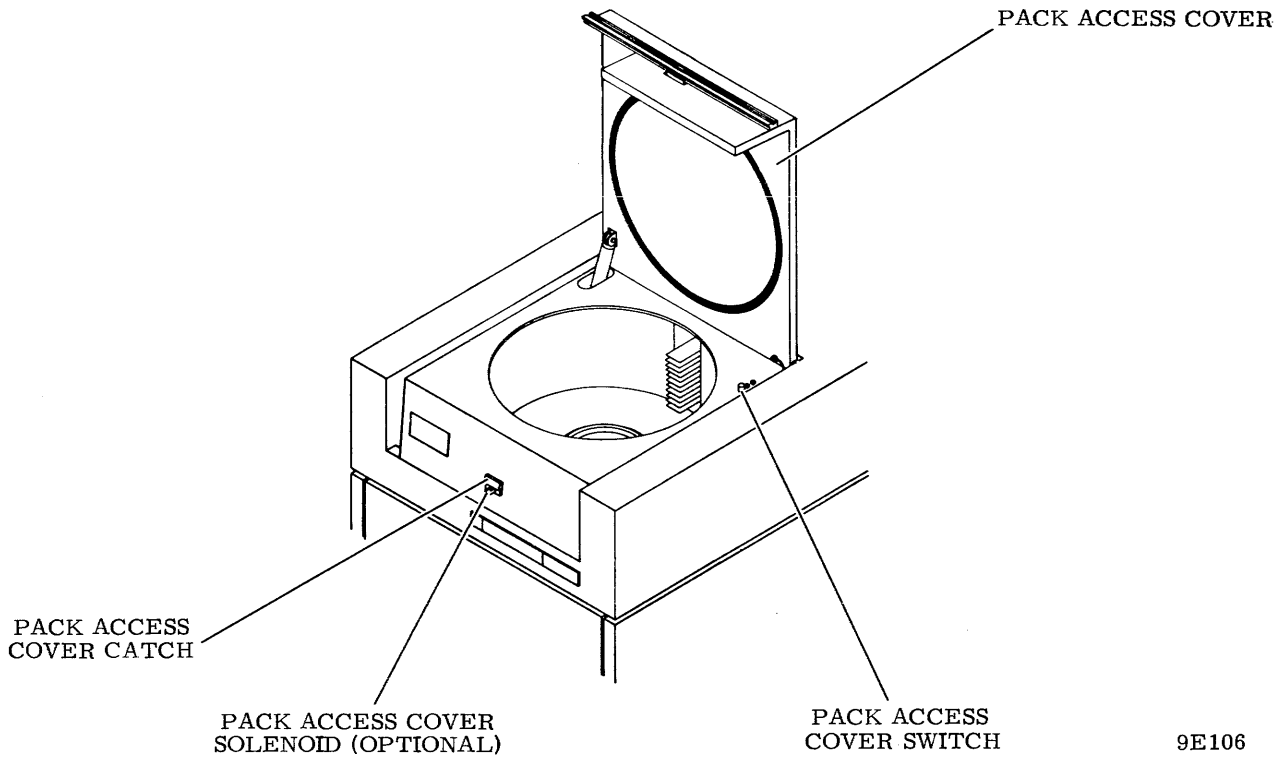


Figure 3-17. Pack Access Cover Switch and Solenoid

The speed sensor logic monitors these signals and uses them to determine if spindle speed is at least 3000 r/min. When this speed is reached, the speed relay is energized; and it remains energized as long as this speed is maintained. However, if spindle speed drops below 3000 r/min the speed relay de-energizes (refer to discussion on Emergency Retract).

Pack On Switch

The disk pack must be securely installed on the spindle for the drive motor to run. This condition is ensured by the pack on switch. The switch is located beneath the spindle (refer to figure 3-18) and is actuated by the lockshaft when the pack is installed.

If the pack is not completely installed, the switch will not be closed and the drive motor will not start. If the pack comes loose during drive operation and the pack on switch opens, the power off sequence is initiated thus stopping the drive motor.

Pack Access Cover Switch

In addition to the pack on switch, the pack access cover switch (refer to figure 3-19) must be closed for the drive motor to run. This switch ensures that the pack access cover is closed.

Opening the switch has the same effect as opening the pack on switch.

Pack Access Cover Solenoid (Optional)

If the drive is equipped with a pack access cover solenoid (refer to figure 3-17), the pack access cover can be opened only if the drive is in a power off condition and the disk pack is not rotating. The solenoid controls the operation of the pack access cover as follows.

When the device is in a power on condition with the pack turning, the solenoid is energized and the solenoid arm is pulled upward. This locks the pack access cover latch and prevents the cover from being opened.

If the drive is in a power off condition with the disk pack stopped, the solenoid is de-energized and the arm drops down. This releases the pack access cover latch and allows the cover to be opened.

HEAD POSITIONING

General

Data is read from and written on the disk by the heads. However, the drive must position the heads over a specific data track on the disk before a read or write operation can be performed. Head positioning is performed by the head positioning mechanism.

This mechanism consists of the actuator, magnet, velocity transducer and heads loaded switch.

The actual positioning is performed by the actuator and magnet. The positioner is controlled by signals received from the servo circuits (refer to discussion on Seek Functions).

The velocity transducer and heads loaded switch provide signals that are used by the servo circuits in controlling head positioning.

Figure 3-18 is a functional block diagram of the head positioning mechanism. The following paragraphs provide further description of the elements shown on this figure.

Actuator and Magnet

General

The actuator and magnet (refer to figure 3-19) work in conjunction to position the heads. The following is a physical and functional description of the actuator and magnet assemblies.

Actuator and Magnet Physical Description

The actuator and magnet are located on the rear half of the deck (refer to figure 3-19).

The actuator consists of the carriage and voice coil both of which are contained in the actuator housing. The carriage is mounted on bearings that allow it to move in a forward or reverse direction along rails attached to the actuator housing. The rear of the carriage forms a cylinder around which the voice coil is wrapped. The heads are mounted on the forward end of the carriage; therefore, the heads, carriage, and voice coil move together as a unit.

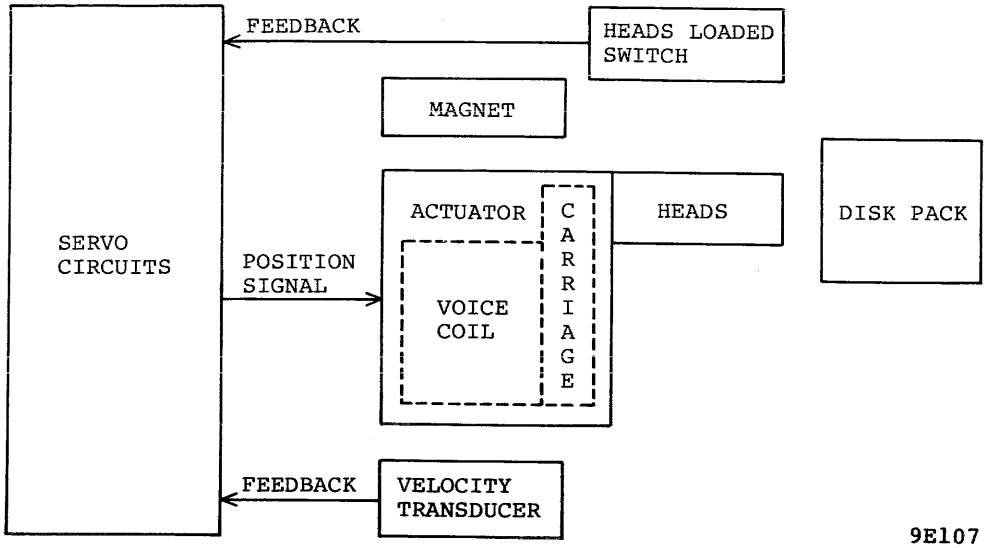


Figure 3-18. Head Positioning Functional Block Diagram

The magnet mounts directly behind the actuator and is a one piece assembly consisting of a large permanent magnet. The magnet contains a circular cutout which allows the voice coil to move in and out of the magnet as the carriage moves.

Actuator and Magnet Functional Description

The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the seek logic and processed; by the power amplifier. The output of the power amplifier is a current signal which is applied to; the voice coil via two flexible insulated metal strips called the voice coil flex leads.

The current from the power amplifier causes a magnetic field around the voice coil which reacts with the permanent magnetic field around the magnet. This reaction either draws the voice coil into the magnetic field or forces it away, depending upon the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

Velocity Transducer

The velocity transducer (refer to figure 3-20) mounts within the magnet and consists of a stationary coil and a movable magnetic core. The core is contained within the coil and connects to the carriage via an extension rod. Therefore, when the carriage moves, the motion is transferred via the extension rod to the core.

When the carriage and core move, an EMF is induced in the coil. The amplitude of this EMF varies directly with the velocity of the carriage and the polarity of the EMF depends on the direction of carriage motion.

The output of the velocity transducer is sent to the servo logic which uses it to control the acceleration of the carriage during seek operations.

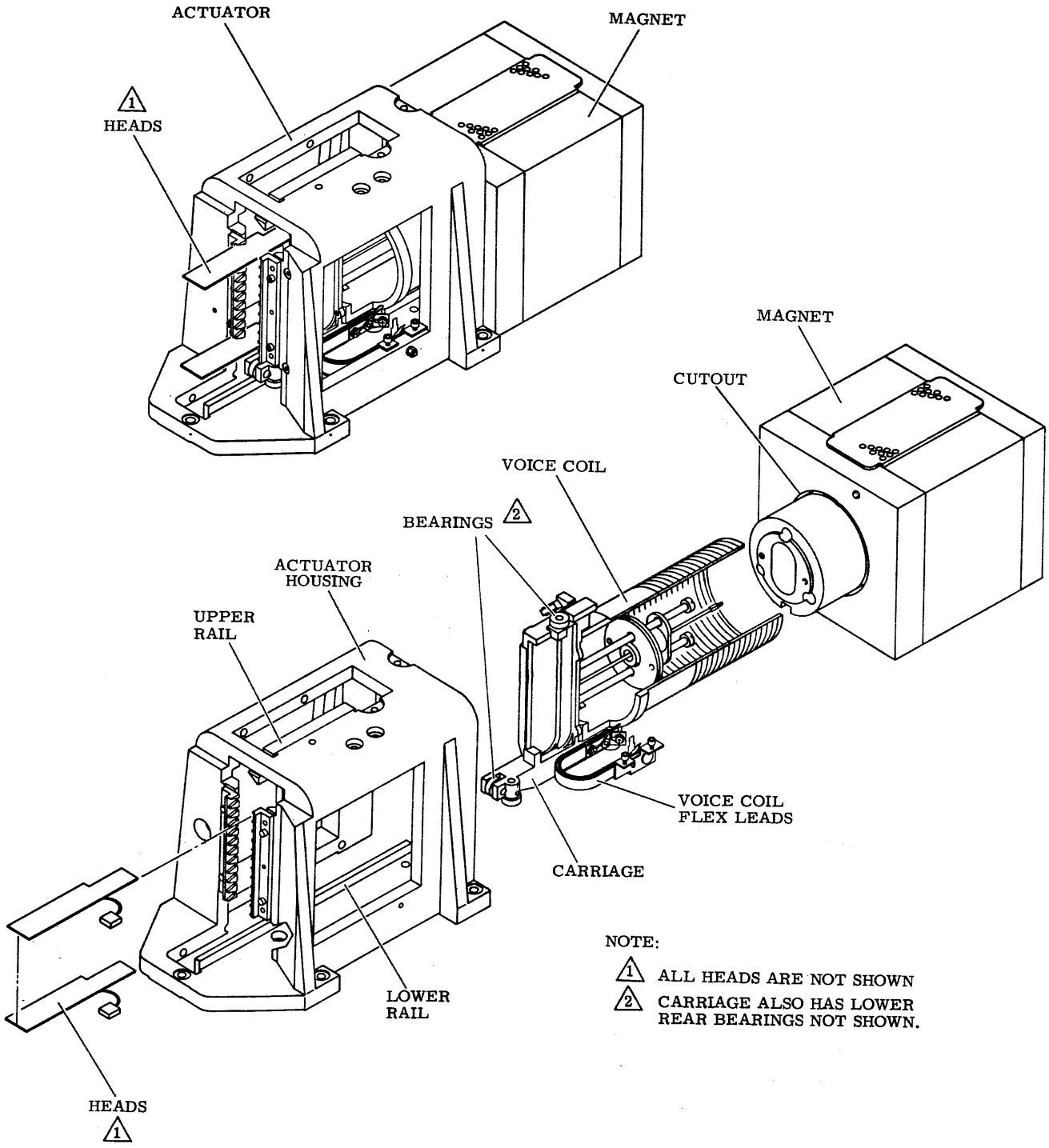


Figure 3-19. Actuator and Magnet Assembly

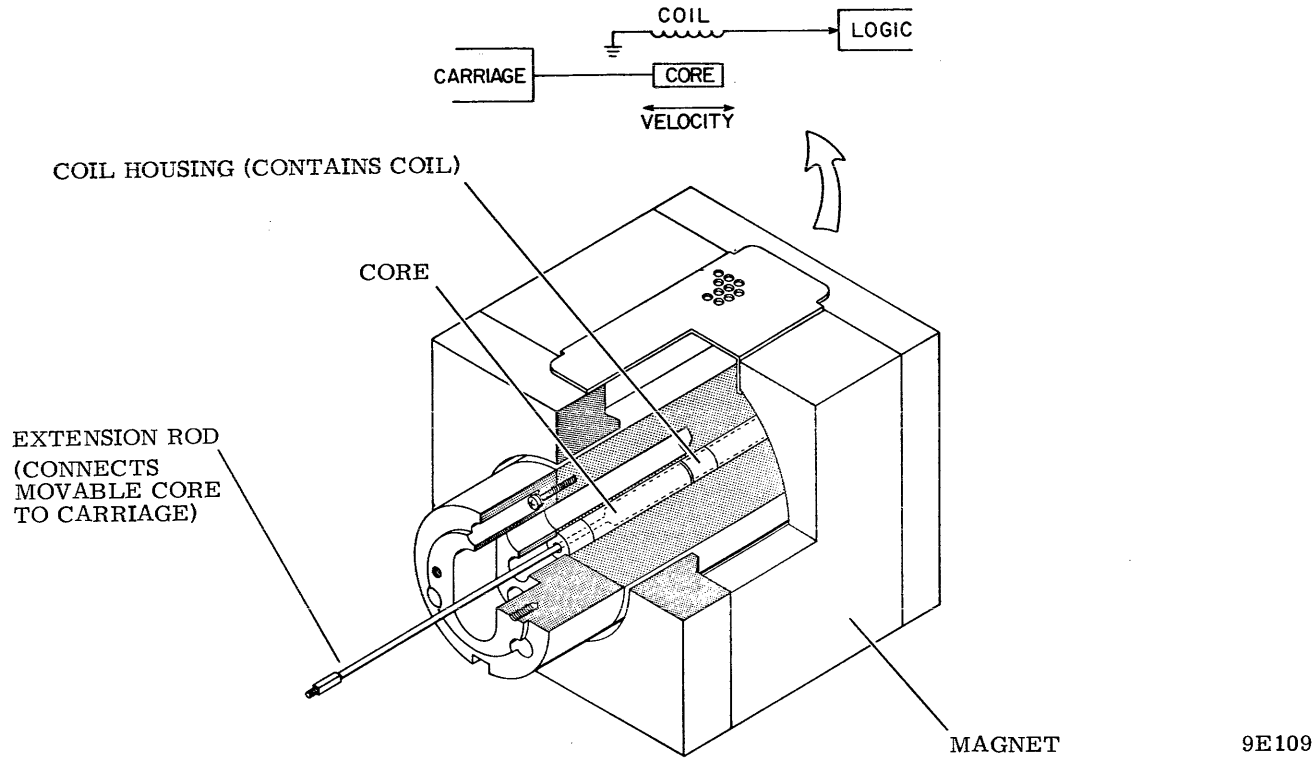


Figure 3-20. Velocity Transducer Assembly

Heads Loaded Switch

The heads loaded switch (refer to figure 3-21) mounts in the actuator housing and indicates whether the heads are loaded or unloaded. This information is used by the seek logic and power on/off sequencing circuits.

The switch is actuated by the carraige as the heads are loaded (moved out over the disk surfaces) or unloaded (moved clear of the disk surfaces and pack area). The switch indicates an unloaded status when the carriage is fully retracted and the heads are clear of the pack area.

During a load sequence, the carriage moves forward from the retracted stop and transfers the switch, to indicate a loaded condition, just as the heads are about to enter the pack area.

During an unload sequence, the carriage retracts and transfers the switch, to indicate an unloaded condition, just as the heads leave the pack area.

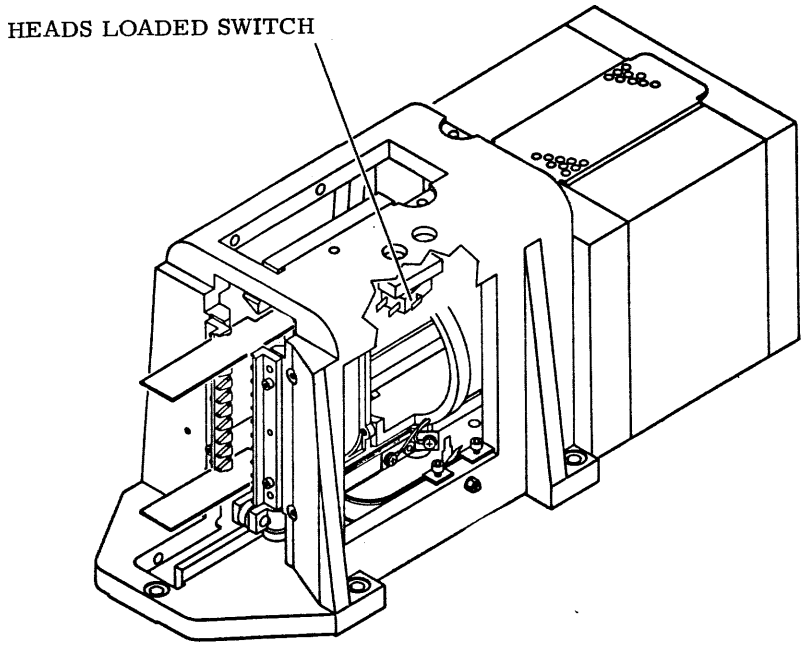
HEADS

General

The heads are electromagnetic devices that record data on and read it from the disk pack. They are mounted in the end of a supporting arm and head and arm together are called a head-arm assembly. The head-arm assemblies attach to the carriage (refer to figure 3-22).

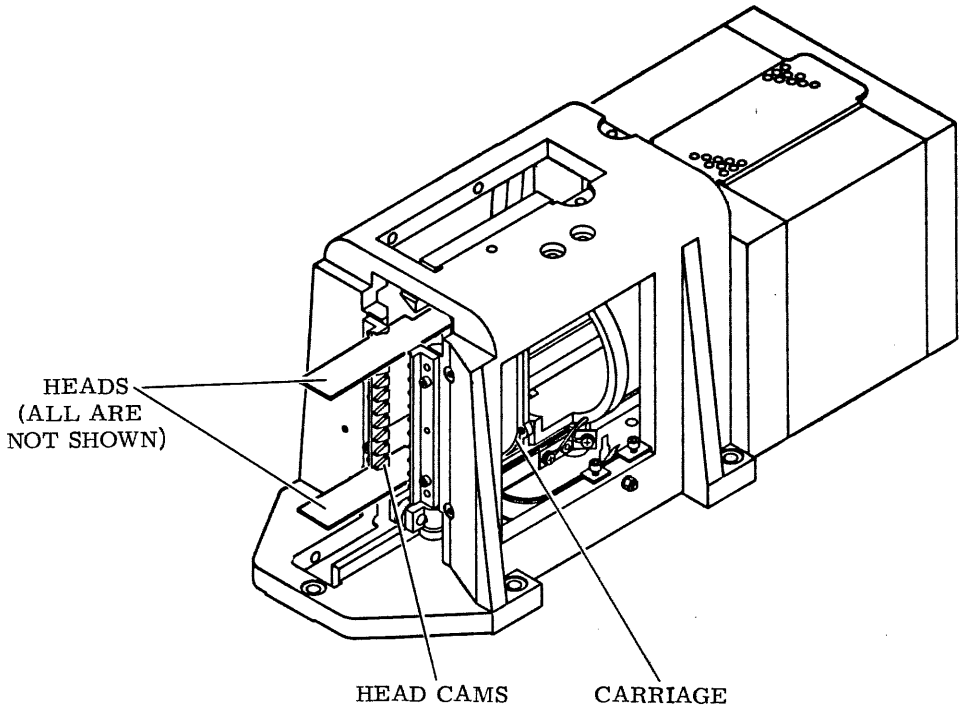
The drive has 20 heads, one for each disk surface. There are two types of heads (1) read/write and (2) servo. There are 19 read/write heads which are used to record data on and read it from the data surface. There is one servo head which is used to read information from the servo surface. This information is used by the drives servo circuits.

The following describes the physical characteristics of the head-arm assemblies and also how they function during head load and unload sequences. Further information concerning the heads is found in the discussions on read/write and seek functions.



9E110

Figure 3-21. Heads Loaded Switch Assembly



9E111

Figure 3-22. Heads

Head-Arm Assemblies Physical Description

Each head-arm assembly consists of a rigid arm, heads load spring, gimbal spring, and the head (refer to figure 3-23).

The rigid arm is mounted on the carriage and causes carriage motion to be transmitted to the head. However, the arm does not provide the action necessary for the head to load, unload and follow the disk surface. This action is provided by the head load and gimbal springs.

The head load spring attaches to the rigid arm and is the mounting point for the gimbal spring. The head in turn attaches to the gimbal spring.

During head loading and unloading, the head load springs ride on the head cams and keep the heads from contacting one another. When the heads are loaded, the head load and gimbal springs work together and allow the heads to move independently of the rigid arms in the directions shown in figure 3-23. Such motion is necessary because when the heads are over the disk surfaces they do not contact the disk but actually fly on a cushion of air created by the spinning of the disk pack.

Information is sent to and from the heads via the head-arm cables. One end of each cable connects to a head and the other end has a plug which connects to a card in the read/write chassis.

Head Loading

The heads must be loaded before the heads can be positioned to a data track for the recording and reading of data. Loading the heads consists of moving them forward from their retracted (unloaded) positions until they are over the disk surfaces. All heads are loaded simultaneously.

The load sequence is initiated during the power up sequence when the disk pack has reached 3000 r/min. At this speed the spinning disk creates a sufficient cushion of air to allow the heads to fly.

When the pack is up to speed and the load logic is enabled, the heads move forward with the head load springs riding on the head cams. As the heads move out over the disk surfaces, the head load springs ride off the surfaces of the head cams (refer to figure 3-24).

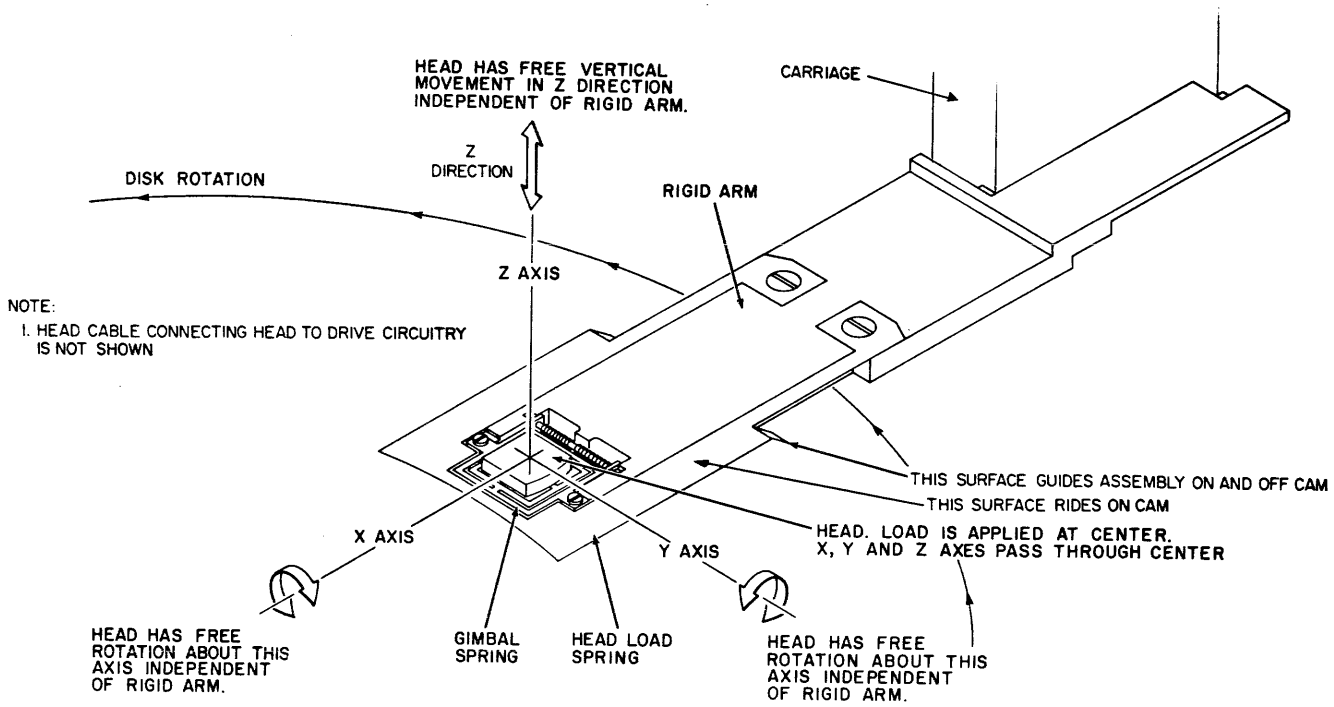


Figure 3-23. Head-Arm Assembly

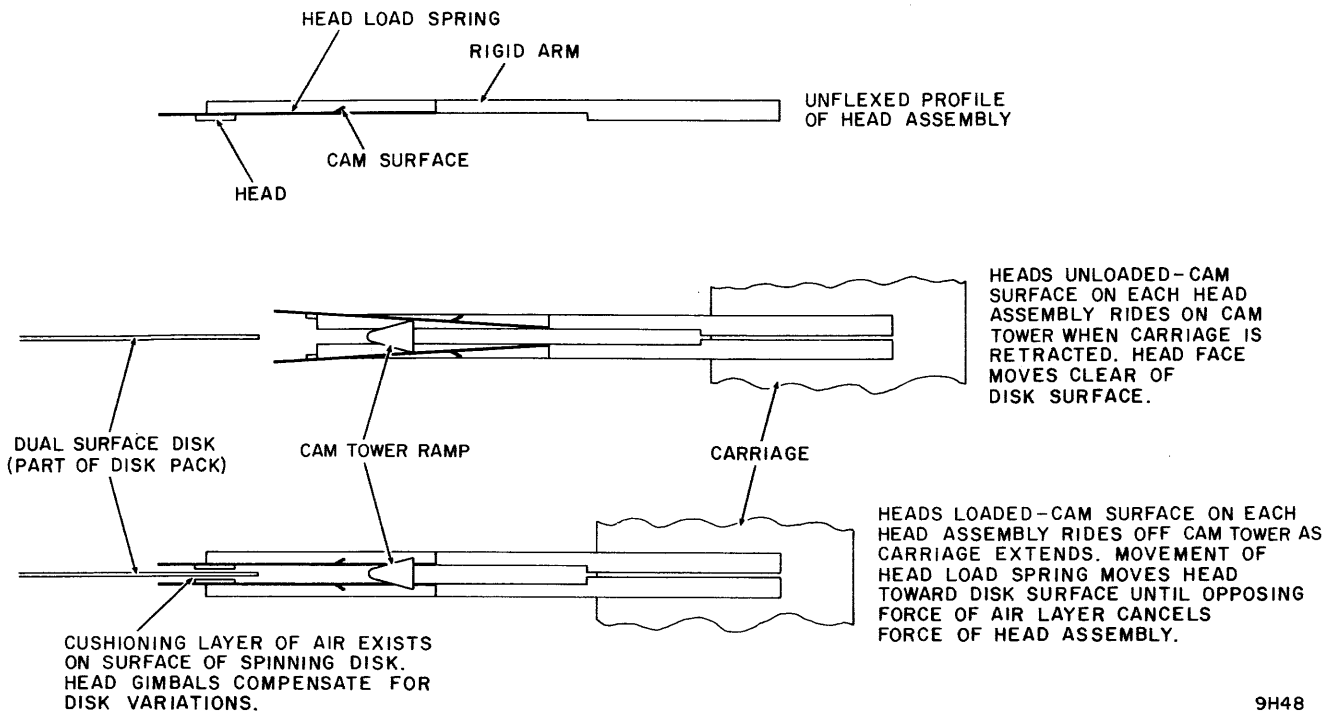


Figure 3-24. Head Loading

The load springs, while riding off the cams, unflex and force the heads toward the air cushions on the spinning disk surfaces. When the cushions of air are encountered, they resist any further approach by the heads. However, the head load springs continue to force the heads down until the opposing air and spring pressures are equal.

The air cushion pressure varies directly with disk speed and if the disk pack is rotating at the proper speed, the air and spring pressures should be equal when the heads are flying at the correct height above the disks.

If the disk pack drops below this speed, air cushion pressure decreases and the head load springs force the heads closer to the disks. Sufficient loss of speed causes the heads to stop flying and contact the disk surfaces. This is called head crash and can cause damage to both the head and disk surfaces.

Because insufficient disk speed causes head crash, loading occurs only after the disk pack is up to speed. For the same reason, the heads unload automatically if disk pack speed drops below a safe operating level (refer to discussion on emergency retract).

Head Unloading

The heads must be unloaded whenever the pack is stopped or if it is spinning too slowly to fly the heads. Unloading consists of retracting the heads until they are no longer over the disk surfaces.

The unload sequence is initiated either during a normal power off sequence, or during an emergency retract function. In both cases current is applied to the voice coil that causes the carriage to move back towards the retracted stop.

As the carriage retracts, the head load springs encounter the head cam surfaces and the heads are pulled away from the disk surfaces. The carriage continues to move back until it is fully retracted.

AIR FLOW SYSTEM

The air flow system (refer to figure 3-25) provides ventilation and cooling air for the drive.

The heart of the air flow system is the blower assembly. This assembly consists of the blower motor, absolute filter, input port from primary filter and output ports to the logic chassis, power supply and pack area.

The blower motor provides the pressure needed to draw air into and push it through the system. The system intake port is located beneath the rear of the cabinet. This port is covered by the primary filter which keeps large particles from being drawn into the system. Air flows from the intake port through a duct in the floor of the cabinet to the blower motor.

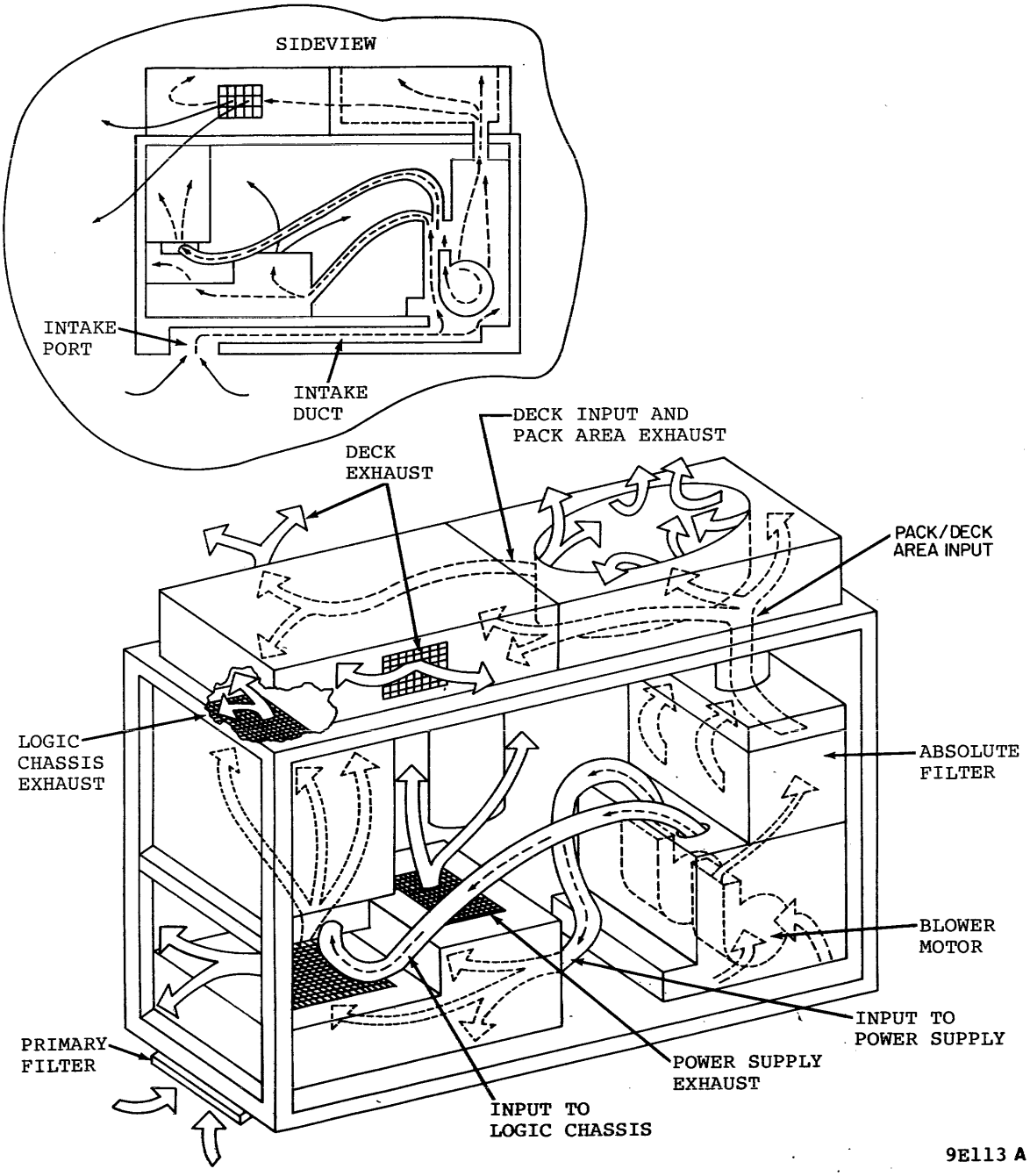


Figure 3-25. Air Flow System

The blower motor forces the air to the power supply, logic chassis, pack area and deck areas. The air to the logic chassis and power supplies, flows through hoses connected between these assemblies and the blower assembly. The air exhausted by the power supply and logic chassis circulates through the lower part of the drive cabinet and provides cooling air for the spindle motor.

The air to the pack area is filtered by the absolute filter which removes particles that might cause damage to the pack or heads. The air is forced into the pack area from all sides causing a positive pressure. This results in an upward dispersion of air, thus preventing the entrance of contaminated air through the pack access cover.

The air intake for the pack area is also forced into the deck area through vents in the rear of the shroud. This air cools the deck components and exits through vents on each side of the deck cover.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals and read/write data transmitted and received by the drive.

The drive comes from the factory as either a single or dual channel unit (refer to discussion on equipment configuration in section 1 of this manual). The single channel units can connect to and communicate with one controller. The dual channel units can connect to and communicate with two controllers (refer to figure 3-26).

The interface, in both cases, consists of the I/O cables and the logic required to carry and process the signals sent between drive and controller (or controllers).

The following describes both the I/O cables and I/O signal processing.

I/O CABLES

All the signal lines between the drive and controller are contained in two I/O cables. They are referred to as the A and B cables. In the case of dual channel units the drive has separate A and B cables to each controller.

The A cable contains lines connected in twisted pairs, which carry commands and control information to the drive and status information to the controller. The maximum number of signal lines varies depending on machine configuration (refer to discussion on equipment configuration in section 1 of this manual).

The B cable contains lines that are either shielded or connected in twisted pairs. These lines carry read/write data, clock, and status information between drive and controller. Figure 3-27 shows all lines (excpet those not used) in the A and B cables. The functions of each of these lines is explained in tables 3-1 and 3-2.

I/O SIGNAL PROCESSING

General

I/O signals from the controller initiate and control all drive operations except power on. The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information, concerning the operation back to the controller via the transmitters. Dual channel units have separate receivers and transmitters for each controller. Figure 3-28 shows the basic logic involved in the routing of I/O signals.

There are two basic types of I/O signals: (1) tag/bus and (2) discrete. The two types differ in that the tag and bus signals work in conjunction to perform a variety of functions while generally the discrete signals work independently each performing a specific function. Both types are described in the following.

Tag/Bus Signals

All commands (except unit select) are sent to the drive via the tag and bus signal lines. The tag lines define the basic operation to be performed and the bus lines modify or further define the basic operation.

Tables 3-1 and 3-2 explain all the tag/bus commands recognized by the drive.

Discrete Signals

In addition to the tag/bus signals, there are various discrete signal lines going between drive and controller. These lines carry clock, status, control and read/write data signals. The function of each of the discrete lines is also explained in tables 3-1 and 3-2.

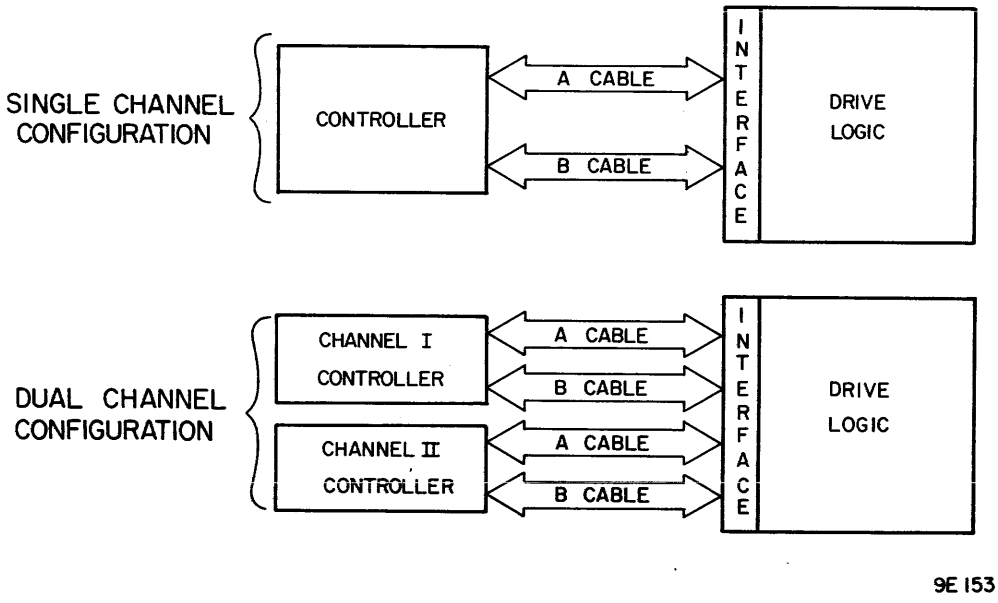


Figure 3-26. Single/Dual Channel Configurations

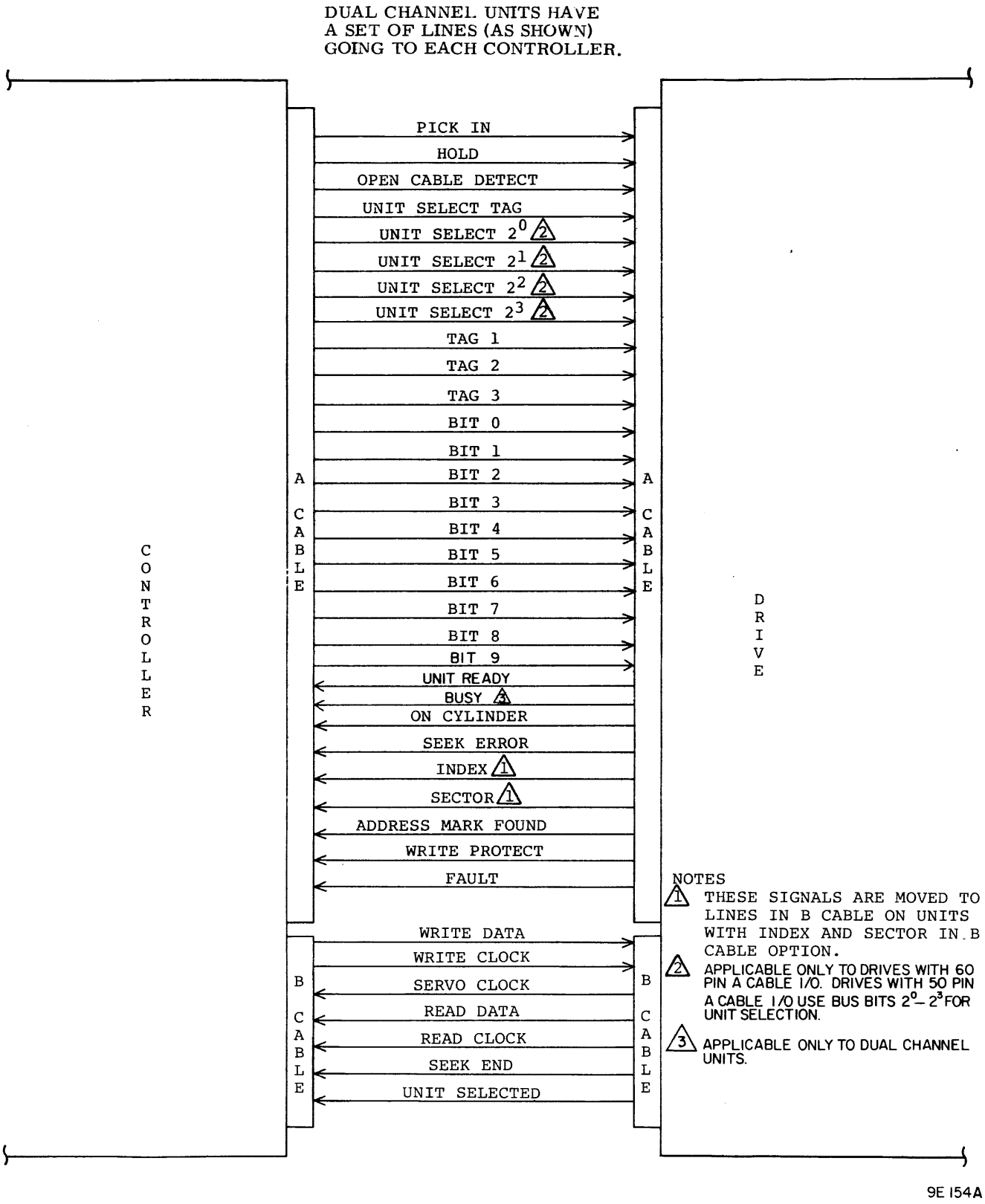


Figure 3-27. Interface Lines

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS

<table>
<tr><th>Signal</th><th>Function</th></tr>
<tr><td>Pick In</td><td>Used for power sequencing. A ground on this line power up drive if LOCAL/REMOTE switch is in REMOTE and START switch is on when drive is up to speed (spindle reaches 2700 r/min). The ground is passed on to the next drive as Pick out (Pick out is terminated as last drive in daisy chain). If Local/Remote switch is in local, this drive is always grounded and therefore Pick out is always passed on to the next drive. Refer to discussion on Power System for more information.</td></tr>
<tr><td>Hold</td><td>Used for power sequencing. This line must be grounded at controller for drive to complete and hold remote power up sequence (refer to discussion on Power System).</td></tr>
<tr><td>Open Cable Detect</td><td>Inhibits Unit Selection and any unwanted command such as Write Gate when "A" cable is disconnected or controller power is lost.</td></tr>
<tr><td>Unit Select Tag</td><td>Initiates unit select sequence and in dual channel units it also reserves drive to that controller provided unit selection is successful (refer to discussion on Unit Selection).</td></tr>
<tr><td>Unit Select lines 2^0 - 2^3 (Not applicable to units with 50 pin A cable I/O).</td><td>Used to select the drive. The binary code on these lines must match the code of the drive logical address plug for the drive to be selected. These lines are used in conjunction with the Unit Select Tag (refer to discussion on Unit Selection).</td></tr>
<tr><td>Tag 1 (Cylinder Select)</td><td>Initiates seek functions and used in conjunction with Bus Bit lines. This tag strobes the cylinder address, contained on Bus Bits lines, into drive logic. Drive must be on cylinder before this tag is sent. Bus Bits are interpreted as follows:
<table>
<tr><th>Bus Bit</th><th>Function</th><th>Bus Bit</th><th>Function</th></tr>
<tr><td>0</td><td>Cyl Adrs 2^0</td><td>6</td><td>Cyl Adrs 2^6</td></tr>
<tr><td>1</td><td>2^1</td><td>7</td><td>2^7</td></tr>
<tr><td>2</td><td>2^2</td><td>8</td><td>2^8</td></tr>
<tr><td>3</td><td>2^3</td><td>*9</td><td>Cyl Adrs 2^9</td></tr>
<tr><td>4</td><td>2^4</td><td></td><td></td></tr>
<tr><td>5</td><td>Cyl Adrs 2^5</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>Tag 2 (Head Select)</td><td>Initiates head select functions and used in conjunction with Bus Bit lines. This tag strobes the head address, contained on bus bit lines, into drive logic. Bus Bits are interpreted as follows:
<table>
<tr><th>Bus Bit</th><th>Functions</th></tr>
<tr><td>0</td><td>Head Adrs 2^0</td></tr>
<tr><td>1</td><td>2^1</td></tr>
<tr><td>2</td><td>2^2</td></tr>
<tr><td>3</td><td>2^3</td></tr>
<tr><td>4</td><td>Head Adrs 2^4</td></tr>
<tr><td>5-9</td><td>Not used</td></tr>
</table></td></tr>
</table>

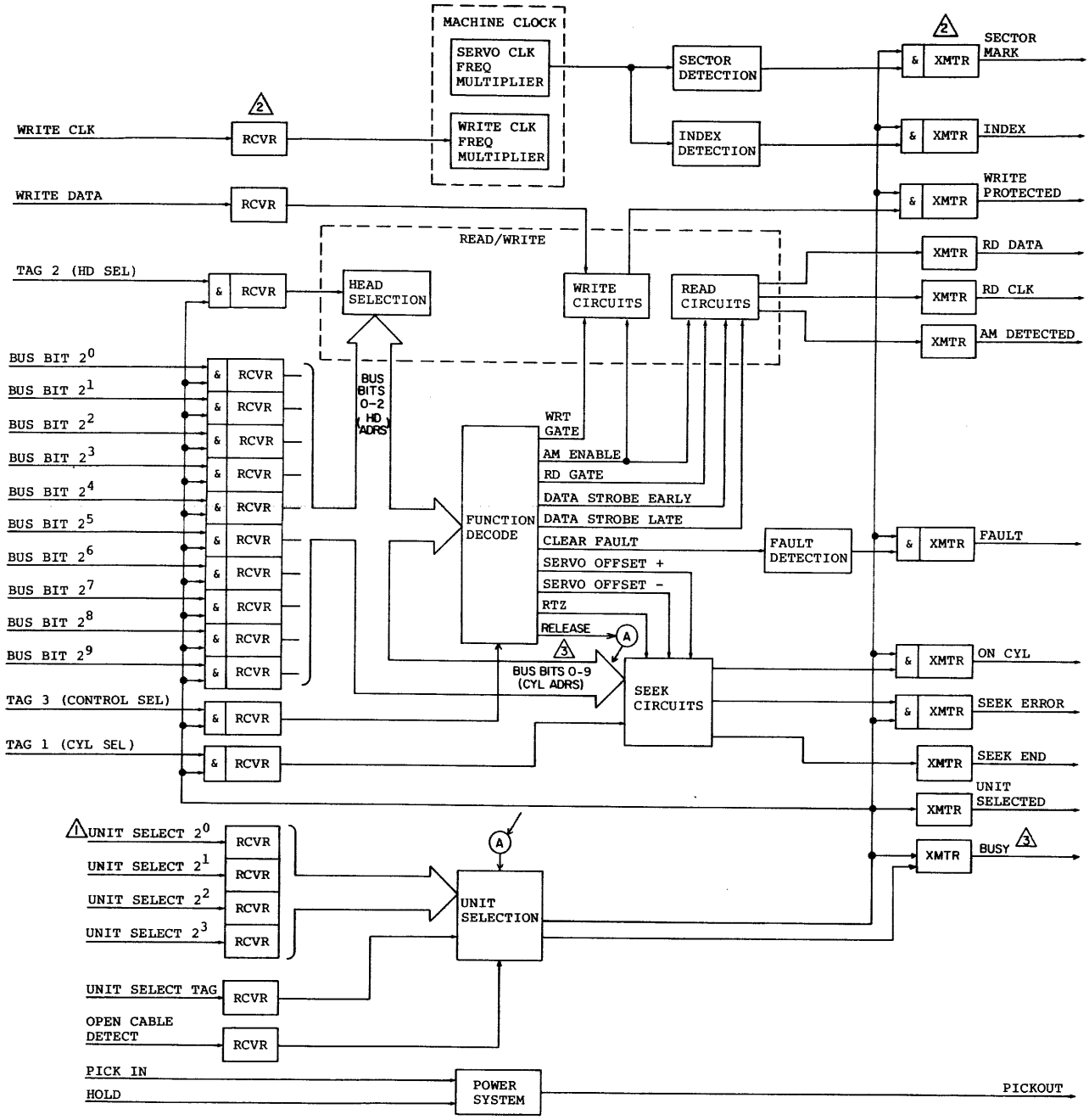
Table continued on next page

Signal Line	Function
Tag 3 (Control Select)	Initiates various operations to be performed by the drive. Used in conjunction with Bus Bit lines and specific operation initiated depends on content of these lines which is defined as follows: **Bus Bit — Function** 0 — Write Gate - Enables write drivers. 1 — Read Gate - Enables the digital read data lines. With PLO option, leading edge triggers read chain to sync on all-zeros pattern. 2 — Servo Offset Plus - Offsets the actuator from the nominal on cylinder position toward the spindle. 3 — Servo Offset Minus - Offsets the actuator from the nominal on cylinder position away from the spindle. 4 — Fault Clear - Pulse sent to drive to clear the fault summary flip-flop. 5 — Address Mark Enable - When combined with a Write Gate, Address Mark is written. When combined with a Read Gate, an Address Mark search is initiated. 6 — RTZ - Pulse sent to drive to cause actuator to seek to track zero. 7 — Data Strobe Early - Enables the PLO data separator (optional) to strobe the data at a time earlier than optimum. 8 — Data Strobe Late - Enables the PLO data separator to strobe the data at a time later than optimum. 9 — Release - Releases dual channel drives from reserved and/or priority selected condition (refer to discussion on Unit Selection). Not used for single channel drives.
Bus Bits (0 - 9)	Used in conjunction with Tags 1, 2 and 3 (also used with Unit Select Tag on units with 50 pin A Cable I/O).
Write Data	Carries NRZ data to be recorded on disk pack.
Write Clock	Synchronized to NRZ Write Data, it is a return of the Servo Clock. This signal is transmitted continuously.

* Used only on 300 MB drives.

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTIONS

Signal Line	Function
Unit Ready	Indicates that drive is selected, up to speed, heads are loaded and no fault exists.
Busy (applicable only to dual channel units.)	Enabled when a unit selection is attempted but the drive is already reserved by the other controller. This signal is returned, to the controller attempting selection, along with the unit selected signal (refer to discussion on Unit Selection).
On Cylinder	Indicates drive has positioned the heads over a track (refer to discussion on Seek Functions).
Seek Error	Indicates that the unit was unable to complete a move within 500 ms, or that carriage has moved to a position outside recording field. A seek error interrupt also occurs if an address greater than track 822 (410) has been selected. Refer to discussions on Seek Functions for more information.
Index	Occurrs once per revolution of disk pack and its leading edge is considered leading edge of sector zero (refer to discussion on Index Detection).
Sector	Derived from servo surface of disk pack, this signal can occur any number of times per revolution of disk pack. Number of sector pulses occurring depends on setting of switches on card in position A06 in logic chassis (refer to discussion on Sector Detection).
Address Mark Found	Indicates that an Address Mark has been found. Enabled by a combination of Read Gate and Address Mark Enable (refer to discussion on Lock to Data and Address Mark Detect Circuits).
Write Protect	Indicates that drives write circuits are disabled. Is true under following conditions: • Head alignment is being performed • Fault condition exists • Write Protect switch on operator panel is activated
Fault	Indicates that one or more of these faults exist: DC power fault, head select fault, write fault, write or read while off cylinder, and Write Gate during a Read operation (refer to discussion on Fault and Error Detection).
Servo Clock	9.677 MHz clock signals derived from servo track dibits (refer to discussion on Machine Clock).
Read Data	Carries NRZ data recovered from disk pack (refer to discussions on Read/Write functions).
Read Clock	Clock signals derived from NRZ Read Data (refer to discussions on Read/Write functions).
Seek End	Seek End is a combination of ON CYL or SEEK ERROR indicating that a seek operation has terminated. If an address greater than 822 (410 on 150 MB units) cylinders has been selected there will be no change in Seek End status (refer to discussions on Seek Functions). On dual channel units this line can also carry a 27 µs pulse indicating the drive is available for selection (refer to discussion on Unit Selection.
Unit Selected	Indicates that the drive is selected. This line must be active before drive will respond to any commands from controller. However, on dual channel units, if Busy is returned in conjunction with Unit Selected, it indicates the drive is reversed to the other controller and selection was unsucessful (refer to discussion on Unit Selection).



NOTES:

1. DRIVES WITH 50 PIN A CABLE I/O DO NOT HAVE UNIT SELECT LINES AND USE BUS BITS 2^0—2^3 FOR UNIT SELECTION
2. DUAL CHANNEL DRIVES HAVE A SET OF XMTRS AND RCVRS FOR EACH CONTROLLER
3. APPLICABLE ONLY TO DUAL CHANNEL UNITS

Figure 3-28. I/O Signal Processing

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers as well as certain transmitters are not enabled until the drive is selected (this is shown in figure 3-28).

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. The reason for this is that the dual channel units must solve the problem of two controllers trying to select the drive when only one may have it selected at a time.

The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence starts when the controller sends a Unit Select tag accompanied by a logical address on the four Unit Select lines (Bus Bits 2^0 through 2^4 in the case of drives with 50 pin A cable I/O).

When the drive recognizes the Unit Select tag it compares its own logical address (as indicated by the logical address plug) to the address sent by the controller. The drives logical address is determined by the logical address plug which fits into the operator control panel. Depending on the plug used, this address can be any number from 0 to 15. If no plug is used the number is 15.

If the address sent by the controller is the the same as that of the drive, and the Open Cable Detect signal is active (indicating the A cable is connected and controller has power) the drive enables its Selected Compare signal. The Selected Compare signal in turn enables the receivers and transmitters to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller. Figure 3-29 shows the logic involved in single channel unit selection and table 3-3 describes the major elements shown on this figure.

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to and can be selected by either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controller must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

- Select - Logically connects the drive to the controller thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by controller having selection but prevents it from being selected by the other controller.
- Release - Releases drive from reserved condition.
- Priority Select - Allows controller not having selection to force select the drive by disabling the channel to the controller having the drive selected or reserved.
- Maintenance Disable - Allows channel to either controller to be disabled during maintenance.

TABLE 3-3. SINGLE CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element	Function
Compare Circuits	Compares address sent from controller with that of drive logical address plug and provides active output when they are the same.
Logic Plug	Fits into drive operator control panel and determines logical address of drive.
Logic Plug Address Register	Loads address of logic plug when Unit Select Tag is received and applies it to input of compare circuit.
Unit Select Address Register	Loads address sent by controller when Unit Select tag is received and applies it to input of compare circuits.
Maintenance Unit Disable Switch	When in Disable position, it Disables Select Compare signal, thereby preventing drive from being selected (this position is used during maintenance). The switch must be in Normal position for drive to be in normal online condition.

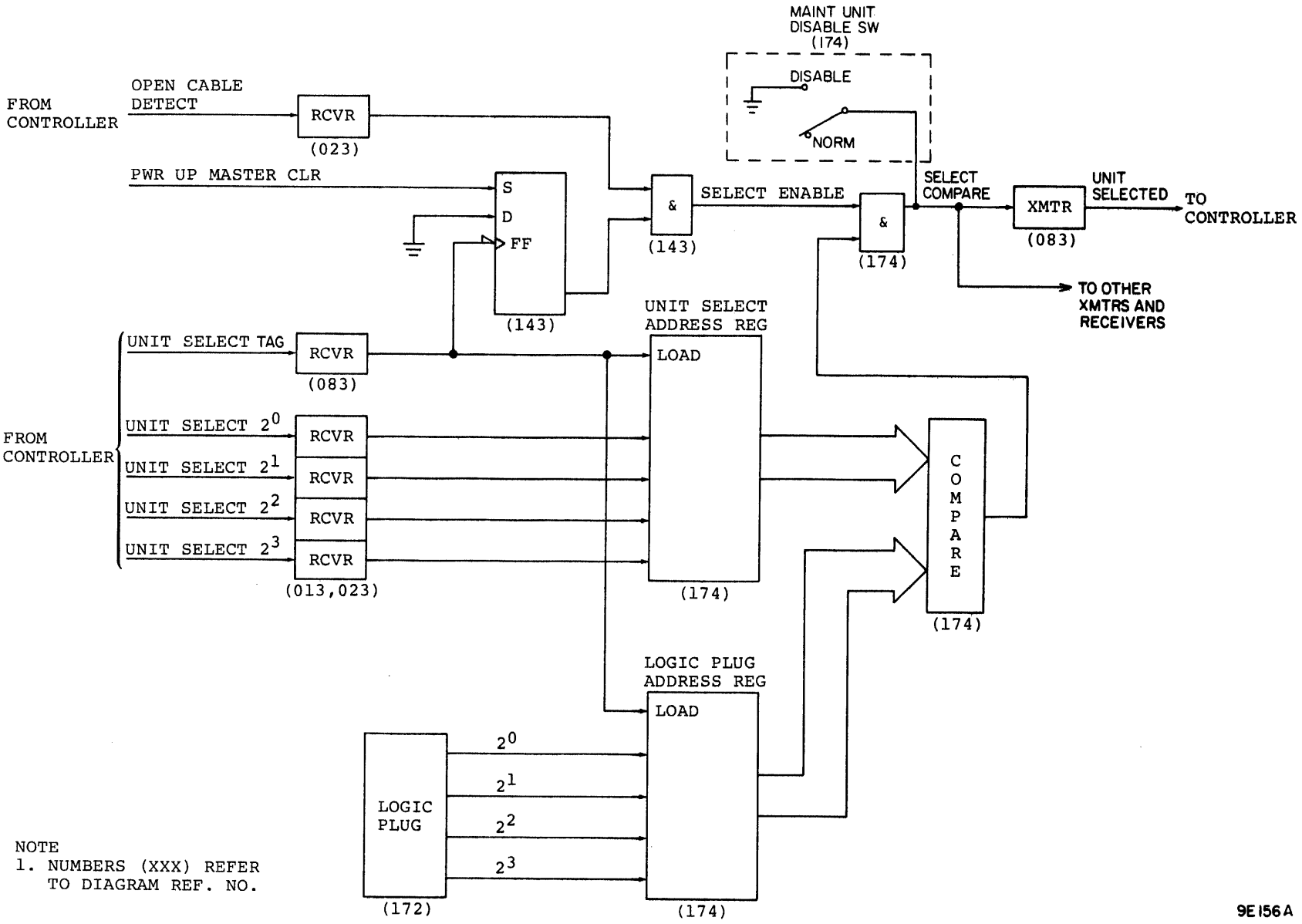


Figure 3-29. Single Channel Unit Select Logic

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, these discussions describe them only as they relate to channel I. Figure 3-30 shows the select logic associated with channel I selection and table 3-4 describes the major elements on this figure. Figure 3-31 is a flow chart of the dual channel unit select functions.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

- Drive is already selected and reserved by other controller.
- Drive is not selected but is reserved by other controller.
- Channel to drive attempting selection has been disabled by either a priority select or maintenance disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

TABLE 3-4. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element *	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or Priority Select command.
Release Timeout One Shot	Deselecting drive causes this one shot to generate a 500 ms (nominal pulse). If drive is in RTM mode the trailing edge of this pulse clears the reserved FF.
Channel I Disable FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Maintenance Unit Disable Switch	Disables channel I whenever it is set to disable position. It must be in NORM position during normal operations.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to Channel I until Channel I releases or Channel II issues a priority Select command.
Channel I Selected FF	Sets during select and reserve sequence and enables transmitters and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see single channel Unit Selection).
Reserved Pulse One Shot	Generates 300 ns pulse whenever either selected FF sets. Leading edge of this pulse clocks Channel I Reserve FF and trailing edge clocks Channel II Reserve FF.
Tiebreaker oscillator	Provides 5 MHz clock pulses for the Channel I and Channel II Selected FFs. Channel I Selected is clocked by leading edge of each pulse thereby giving priority to Channel I in cases where both controllers attempt selection simultaneously.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by channel II, this FF clears and thereby triggers the Select Ready One shot.
Select Ready One Shot	Generates 27 μs pulse whenever either Tried FF clears. This pulse is sent to controllers via the Seek End lines.

* Includes only those elements directly concerning channel I and shown on figure 3-30.

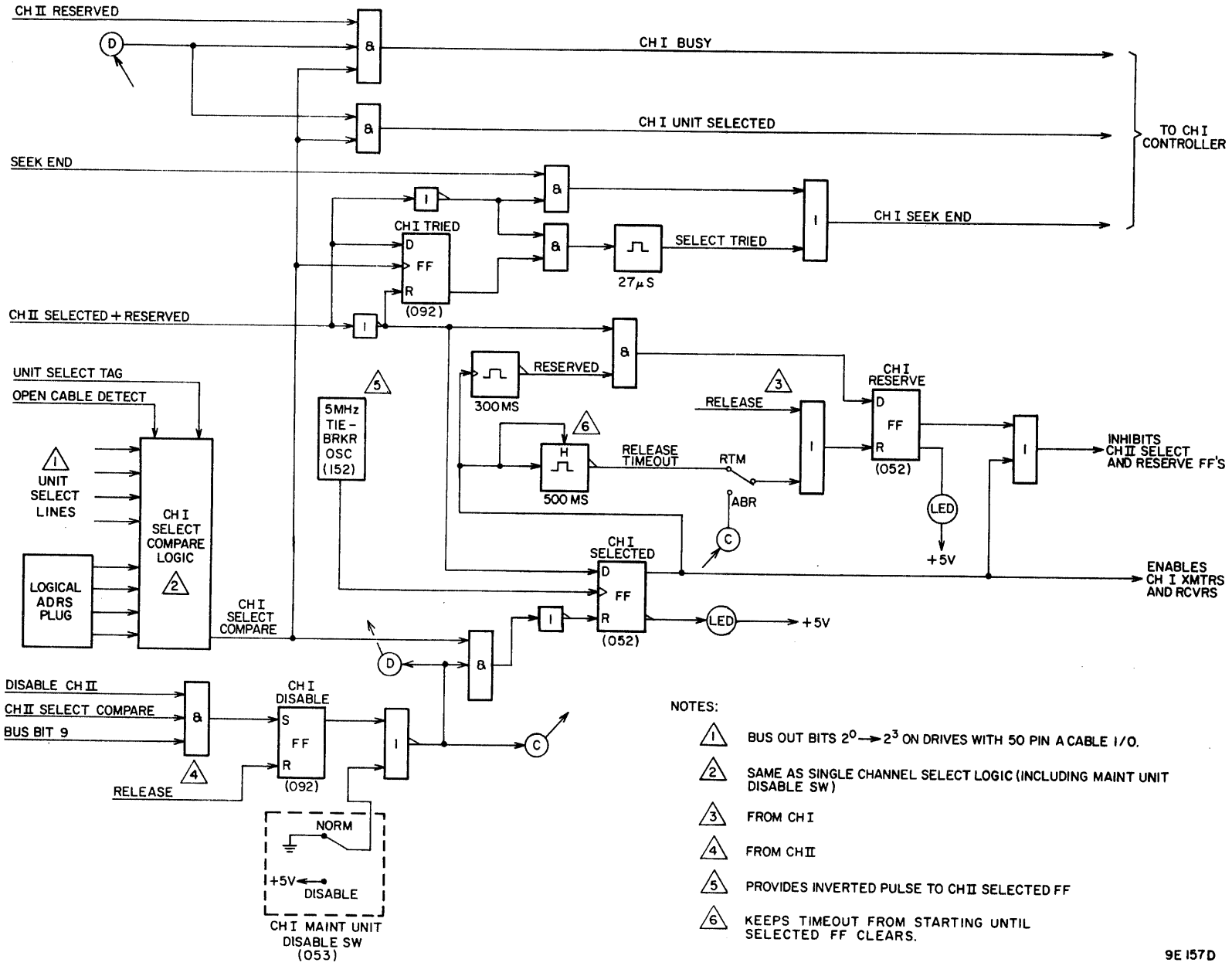


Figure 3-30. Channel I Dual Channel Select Logic

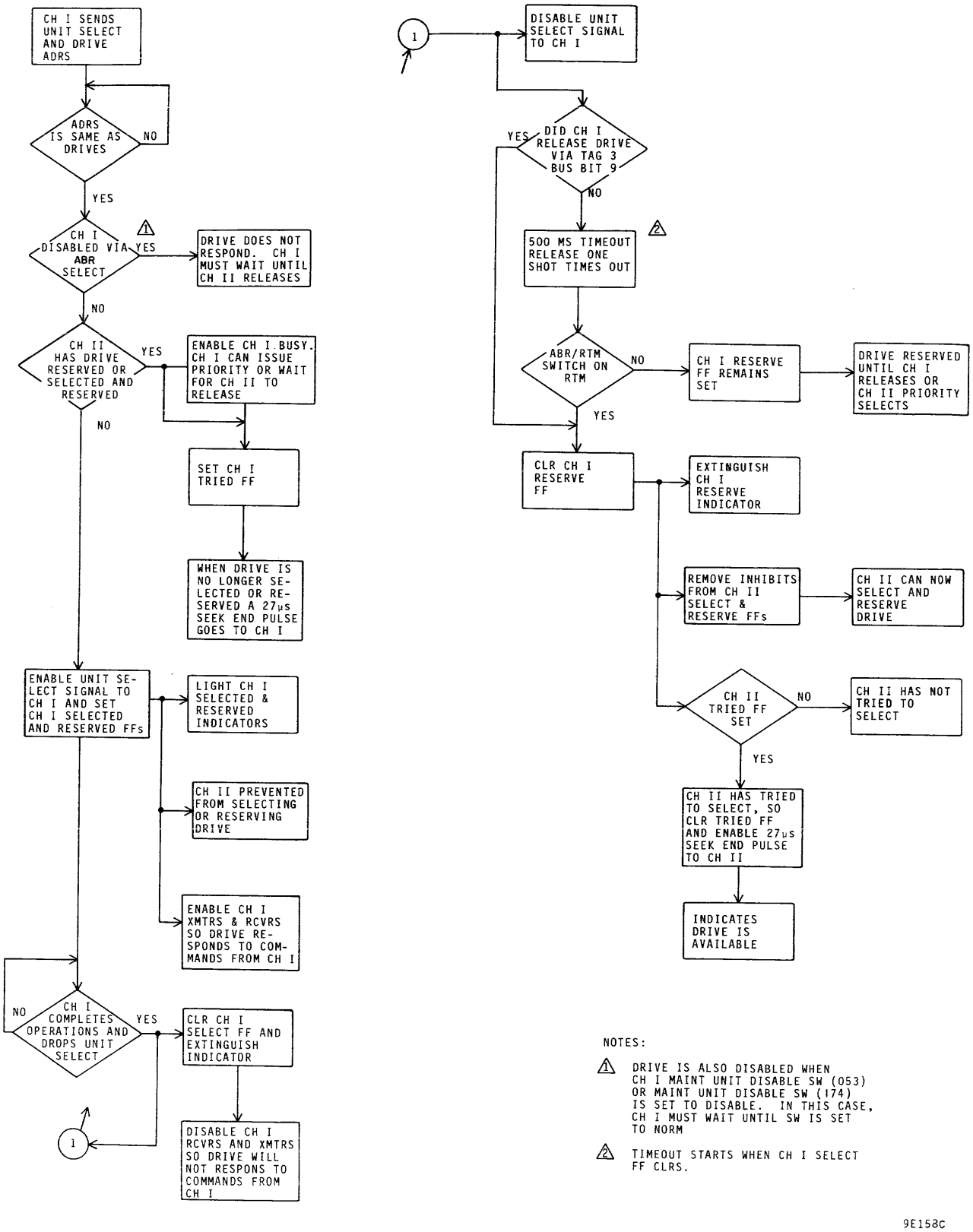


Figure 3-31. Dual Channel Select and Reserve Flow Chart

Assuming the drive is available (not selected, reserved or disabled in a priority selected or maintenance disable) and it receives a Unit Select Tag and logical address from channel I, it compares the address received with that indicated by its logical address plug. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units (refer to figure 3-29).

Enabling Channel I Select causes Channel I Unit Selected to go active and also removes the clear from the Channel I Selected FF. The next 5 MHz tiebreaker clock pulse sets the Channel I Selected FF.

Setting the Channel I Unit Selected FF enables the Channel I receiver and transmitter and triggers the 300 nanosecond reserve one shot. The resulting one shot pulse clocks and sets the Channel I Reserved FF. With the select and reserve FFs set, the sequence is complete and the drive responds to further commands from Channel I.

Provided Channel II does not issue a priority select (see Priority Select Function discussion), the drive remains selected and reserved to channel I until this controller either disables its Unit Selected Tag or changes the logical address. At this time, the drives Channel I selected FF clears thus disabling the transmitters and receivers to that channel. This also disables the Unit Selected signal thus informing the con troller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (thus allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also clear. This is cleared by either a release, priority select, or maintenance disable function (refer to these discussions).

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the Initial Select and Reserve sequence. However the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller; but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is being used by channel II. The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears thereby generating a 27 µs Seek End Pulse to the channel I controller. This informs the controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. It should be noted that the drive must also be in a selected condition (via a Unit Select Tag) when the release is issued. There are two types of release functions (1) timeout release pulse and (2) Release command.

The timeout release pulse is capable of releasing the drive from only the reserved condition. This pulse is generated by the 500 ms Timeout Release one shot and releases the drive by clearing the Reserve FF. The pulse is triggered when the drive is selected (Select FF sets), and times out 500 ms after the drive is deselected (Select FF clears). Whether or not the one shot has any effect on the Release FF, depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one shot times out thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one shot has no effect on the FF and the drive remains reserved.

A Release command releases the drive from both the absolute reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive.

Priority Disable Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Bit 9). This command disables the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the disable.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn clears the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a Release command to clear it.

Maintenance Disable Function

It is possible to disable either channel by setting Maintenance Unit Disable switch for that channel (refer to figure 3-30) to the disable position. It is also possible to disable both channels by setting the Maintenance Unit Disable switch for Select Compare (refer to figure 3-29) to the disable position.

SEEK FUNCTIONS

GENERAL

During seek operations the drive positions the heads over the desired cylinder on the disk pack. The drive servo circuits control this function. The following describes the servo circuits and how they function during various seek operations.

It is divided into the following areas:

- Servo Circuit Operation - Describes the Servo circuit, which controls the voice coil positioner.
- Track Servo Circuits - Explains operation of track servo portion of servo circuits.
- Basic Seek Operation - Provides a general description of how the drive functions during a seek operation.
- Types of Seeks - Describes the different types of seeks performed by the drive.
- End of Travel Detection - Describes what happens when the drive positions the heads beyond the normal area of travel.

These discussions are applicable to both the 300 MB (megabyte) BK7XX and 150 MB BK6XX drives. For the most part, these drives function identically; however, some things (such as seek lengths and cylinder numbers) are diferent and this is noted in the text. For example, the drive seeks to cylinder 822 (410 on 150 MB units). In this case 410 applies only to 150 MB BK6XX units. In all such cases, the note in parenthesis applies to 150 MB BK6XX units.

Figure 3-32 shows the basic elements in the servo circuits and table 3-5 explains their functions. The following discussions explain the servo circuits and seek operations in more detail.

BASIC SERVO CIRCUIT OPERATION

The servo circuits form a closed loop servo system that position the heads as directed by the controller.

The servo system controls the movement by comparing the present position of the heads to the desired future position and generating a position error signal proportional to this distance.

The position error signal is applied to the voice coil causing the heads to move in the desired direction. As the heads move, feedback signals are generated that indicate how fast the heads are moving (velocity) and how far the heads have moved toward the desired position (position feedback).

The loop applies its position and feedback signals to the summing amplifier. If the summation of these signals is not equal to zero, the summing amplifier outputs a signal proportional to the amplitude of the difference voltage (which signifies the amount of displacement from the desired position) and the phase of the difference voltage (which indicates the direction of displacement).

The error output from the summing amplifier is applied to the power amplifier which supplies the current for the voice coil positioner. The voice coil positioner supports and moves the read/write heads. The voice coil is located within a powerful magnet and whenever a current passes through the voice coil windings, the interaction of the induced EMF and the magnet's flux field cause the positioner to move. The acceleration of the motion is proportional to the polarity and amplitude of the voice coil current.

TRACK SERVO CIRCUIT

General

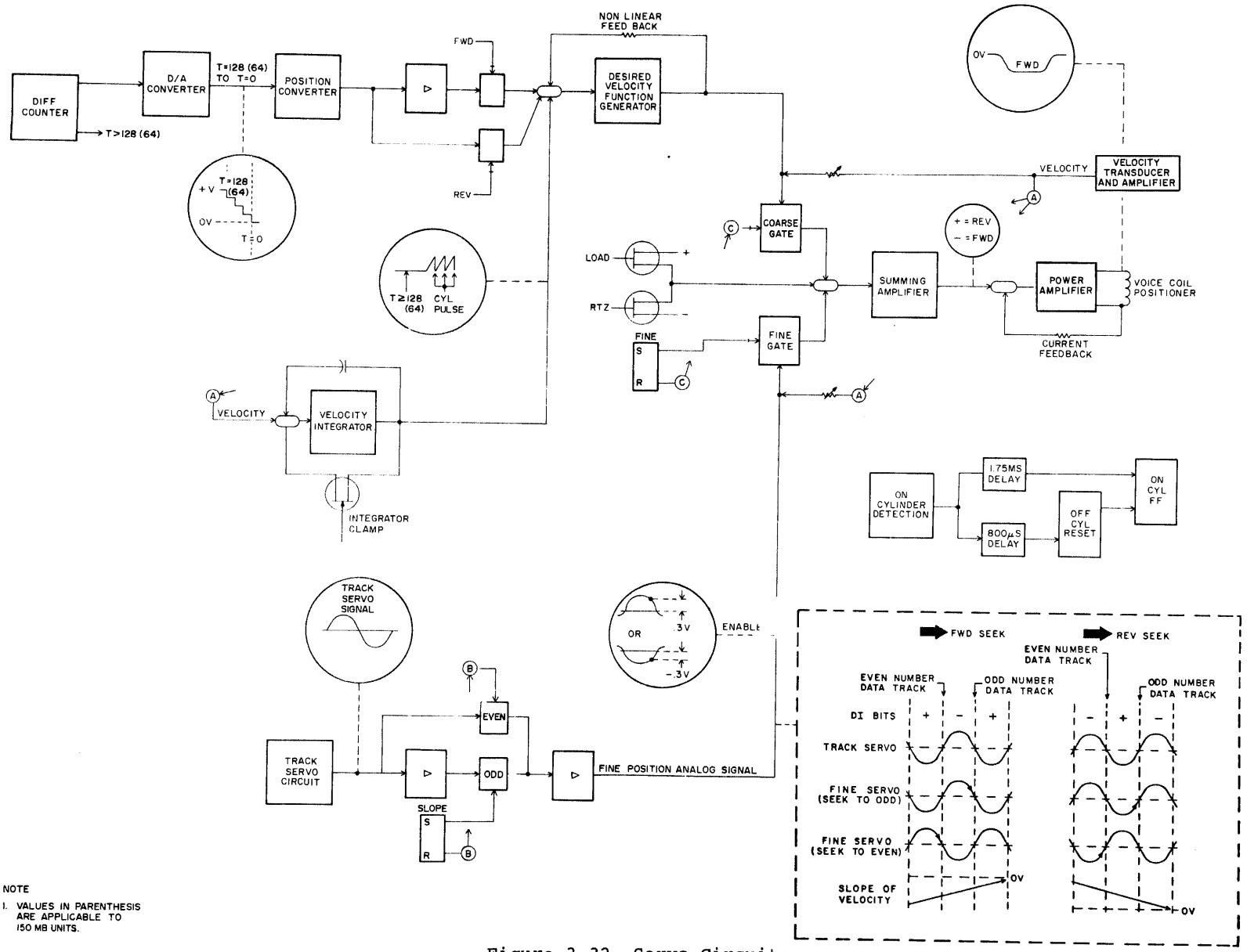
The track servo circuit generates signals used by the servo system to position the heads. These signals are as follows:

- Dibit Signals - Used by the end of travel detection, Index and Machine Clock circuits.
- Track Servo Signals - Indicates displacement of heads from their nominal track centerline.
- Cylinder Pulse Signals - Used by servo circuits to indicate each physical track crossing.

The basic elements of the track servo circuit are shown in figure 3-33 and explained briefly in table 3-6.

Dibit Signals

Information for this circuit is derived from the servo head (figure 3-34). This is physically similar to the read/write heads,



NOTE

1. VALUES IN PARENTHESIS ARE APPLICABLE TO 150 MB UNITS.

Figure 3-32. Servo Circuit

TABLE 3-5. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Cylinder Address Register	Holds the present cylinder address. It is updated to the new cylinder address when a seek is initiated.
Cylinder Address Adder	Combines the present cylinder address with the new cylinder address complement to arrive at the difference.
Difference Counter	Holds the number of logical tracks yet to be crossed before reaching the desired track or cylinder. Counter value is zero when on cylinder.
Digital-to-Analog Converter	Monitors the seven lowest order bits of difference counter to provide an analog indication of Position Error during the last 128 (64 on 150 MB units) logical tracks (except last track) of all Seek operations. The amplitude of the D/A converter output is proportional to the number of tracks to go. Amplitude is clamped at maximum value while logical tracks remaining are equal to, or greater than 128 (64 on 150 MB units). Amplitude decreases in discrete steps (controlled by D/A converter) as last 128 (64 on 150 MB units) logical tracks are crossed. Signal is inverted for reverse seeks.
Desired Velocity Function Generator	Processes D/A converter output at gain levels that vary as Position Error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control to deceleration. The parallel non-linear feedback circuit maintains tight loop control by increasing gain as the Position Error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems. It also minimizes drift about null.
Summing Amplifier	Generates a control signal to drive the power amplifier. When Position Error exceeds Velocity Amplifier signal, control signal causes power amplifier to accelerate carriage. When Velocity signal exceeds Position Error, carriage decelerates.
Load Gate	Provides a constant positive input to the summing amplifier. This causes forward velocity of 7 ips.
RTZ Gate	Provides a constant negative input to the summing amplifier. This causes reverse velocity of 7 ips.
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. Also receives a negative feedback from positioner which acts to cancel current coupling that occurs from the velocity transducer location within the magnetic field created when current is applied to the voice coil positioner. The associated amplifier disable forces amplifier gain to zero during a power off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement to the retraction position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 128 (64 on 150 MB units) track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter.

Table continued on next page

TABLE 3-5. SERVO CIRCUIT FUNCTIONS (Contd)

Circuit Element	Function
Fine Latch	When difference counter is 1 (T=1) and integrated velocity exceeds 1.4v, it indicates that there is one-half physical track to go. Fine latch sets to enable fine gate and disable coarse gate. This switches position error input to summing amplifier from Desired Velocity (coarse gate) to fine position analog (fine gate). Fine also has the following effects: • Turns on integrator clamp to switch off velocity integrator. • Enables on cylinder detection. During load or RTZ sequences, both outputs of Fine Latch are high. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Slope FF	Used to select proper Track Servo signal phase for use as Fine Position Analog signal (signal controlling servo loop as last physical track is approached and carriage is stopped). If this FF is cleared, the seek destination is an even numbered physical track and the track servo signal will not be inverted for use in stopping the carriage. If this FF is set, an odd physical track is identified and track servo is inverted. This FF is always clear on 150 MB drives because it seeks only to even physical tracks.
On Cylinder Detector	Monitors fine position signal when $T \leq 1$. When signal is less than about 0.3v, heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is returned to controller and to drive logic. If heads overshoot at end of seek so that voltage exceeds 0.4v, delay is reinitiated. Delay permits carriage to settle out before controller may attempt any read/write operations.

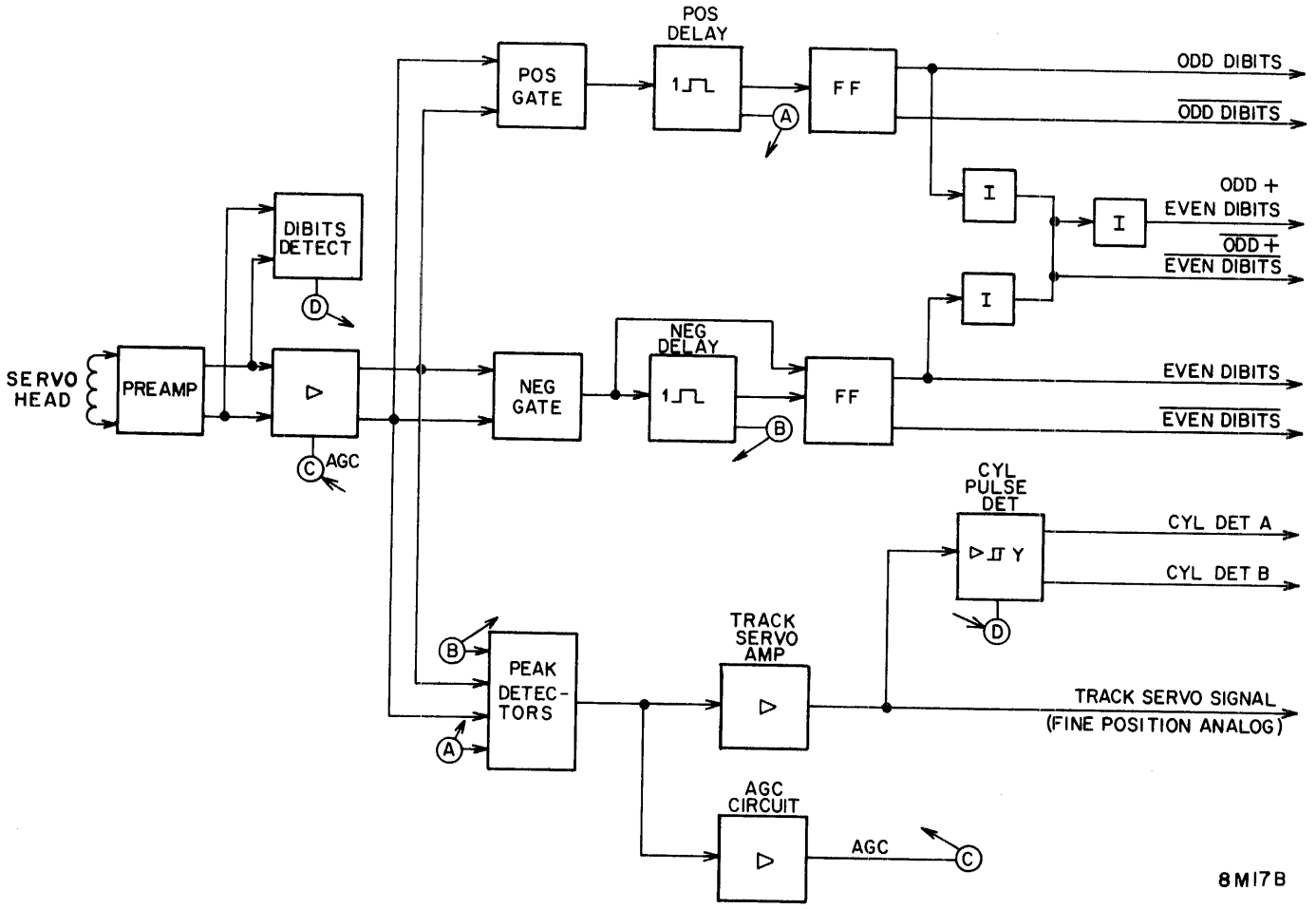


Figure 3-33. Track Servo Circuits

TABLE 3-6. TRACK SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Servo Head	Reads dibit information from the disk servo tracks. This head cannot write.
Track Servo Preamplifier	Amplifies the signal read by the track servo head.
Positive and Negative Gates	Separate dibit waveforms into positive and negative components. Positive gate triggers during first half-cycle of positive dibits (read from odd dibit track) and second half-cycle of negative dibits (read from even dibit track). Negative gate triggers in the reverse condition.
Positive and Negative Delays	Function as synchronizing gates to control dibit pulses generation. Positive delay fires at the leading edge of positive gate. If negative gate output is available before positive delay times out, it indicates that positive dibit has been sensed. This fires the odd dibit one-shot. (Although the positive delay fires during negative dibits, a negative gate is not available immediately thereafter; the odd dibit one-shot is not enabled.) The negative delay functions in the reverse condition. These delays inhibit inputs to peak detectors so that they react only to the positive peaks of their respective dibits.
Even Dibits and Odd Dibits One-Shots	Provide 890-nsec pulses indicating dibits. Frequency of each one-shot is 403 kHz.
Peak Detectors	Provide peak detection of dibit signals. Outputs are proportional to dibit amplitudes: the greater the amplitude, the more negative the output. When head is centered between dibit tracks, outputs of + and - integrators are equal. As head moves from centered position, output from one integrator increases negatively while output from the other integrator becomes less negative. The difference between these two outputs is proportional to servo head displacement from centered (on cylinder) position.
AGC Circuit	AGC voltage is proportional to sum of dibit signals. As signal strength increases, voltage goes less negative to reduce circuit gain.
Heads Loaded Detection	Provides positive signal when dibit amplitude is sufficient to indicate that heads are loaded over dibit tracks. Prior to this high output, positive/negative gates are inhibited to indicate no servo tracks detected. If dibits are not available within 350 ms after start of Load sequence (or if lost for 350 ms at any other time), no servo tracks FF sets. This initiates an RTZ sequence to unload heads and sets fault FF.
Track Servo Amplifier	Provides signal proportion of sum of + and - peak detectors. Output is null when head is centered between dibit tracks (on cylinder); negative when over odd track or outer guard band; positive when over even track or inner guard band.
Cylinder Pulse Detection	Provides cylinder pulses to difference counter and other logic elements as track servo signal approaches null. One pulse is generated per track crossed (even/odd transition or odd/even transition).

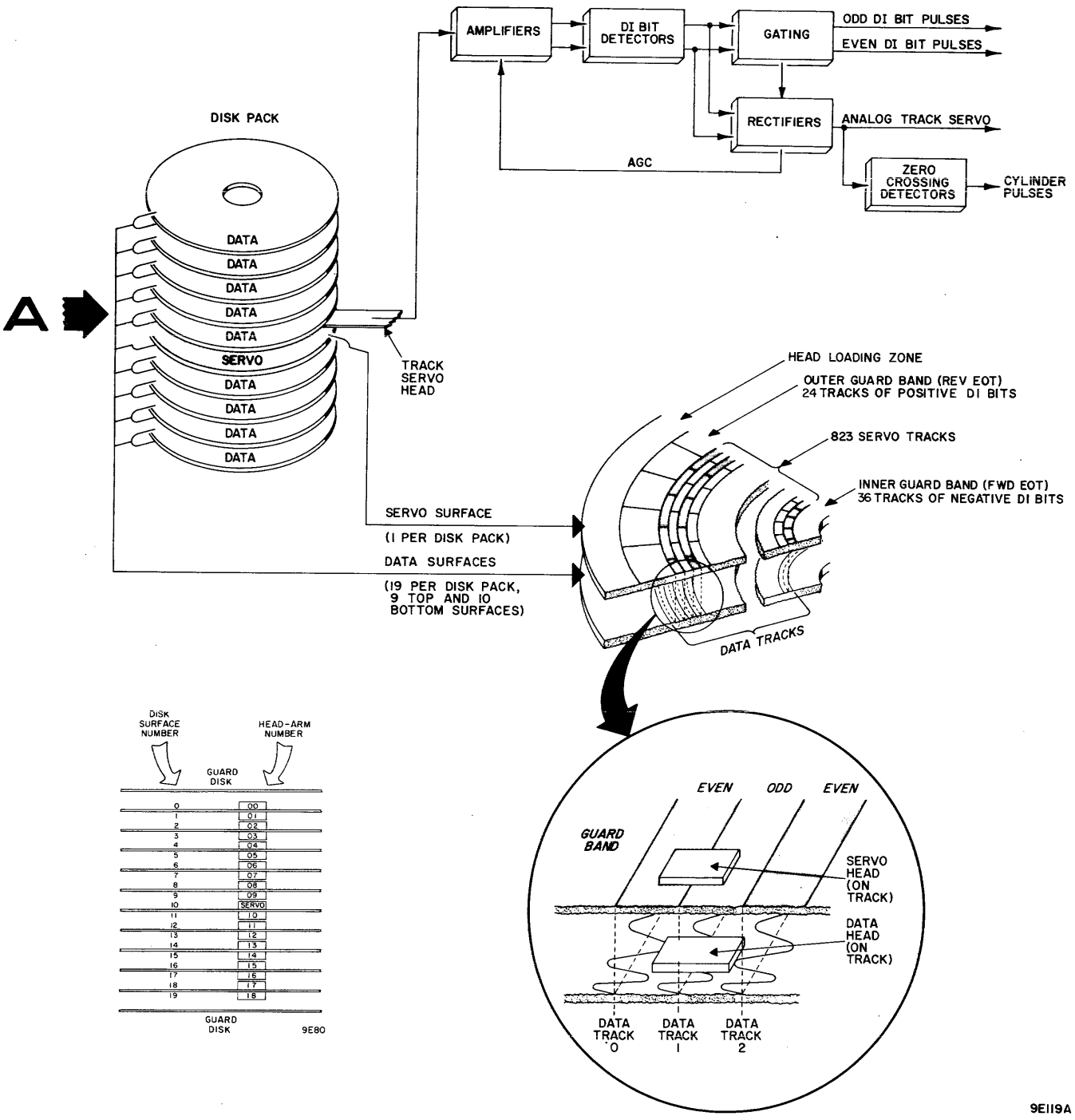


Figure 3-34. Servo Surface Format

except that it does not write. The head reads information from the servo track surface of the disk pack. This information is known as dibits; dibit is a shortened term for dipole bit. Dibits are prerecorded on the servo surface during manufacture of the disk pack. Do not confuse the servo surface with the disk pack recording surfaces.

Dibits are the result of the manner in which flux reversals are recorded on the servo tracks. One type of track, known as the Even track, contains negative dibits. The other track, the Odd track, contains positive dibits.

There are 883 dibit tracks on the servo surface. At the outer edge of the surface is a band of 24 positive dibit tracks. This area is the Reverse End of Travel (EOT) or outer guard band. Then, there are 823 servo dibit tracks alternately recorded with negative and positive dibits. Finally, toward the inner edge of the pack, there are 36 tracks containing only negative dibits. This is the Forward EOT or inner guard band.

When the read/write heads are located at the centerline of a data track, the track servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position, the amplitude of one dibit component increases while the other decreases. This error voltage is the track servo signal.

After being differentially amplified, the track servo signal is applied to gates that separate the dibit signals by sensing the positive and negative flux reversals (figure 3-35). A positive dibit consists of a positive-going waveform immediately followed by a negative-going waveform. This component triggers the Odd Dibits FF. On the other hand, a negative dibit consists of a negative-going waveform followed immediately by a positive-going waveform. This component triggers the Even Dibits FF.

Track Servo Signal Generation

The track servo signal indicates the displacement of the servo head from the on-track position. When the head is centered between dibit tracks, this signal is at a null. It swings in the positive direction when the amplitude of the even (negative) dibits being sensed exceeds the amplitude of the odd (positive) dibits, and vice-versa. Amplitude is maximum when the head is centered over one dibit track, that is, the head is at its maximum distance from the centerline of the data track.

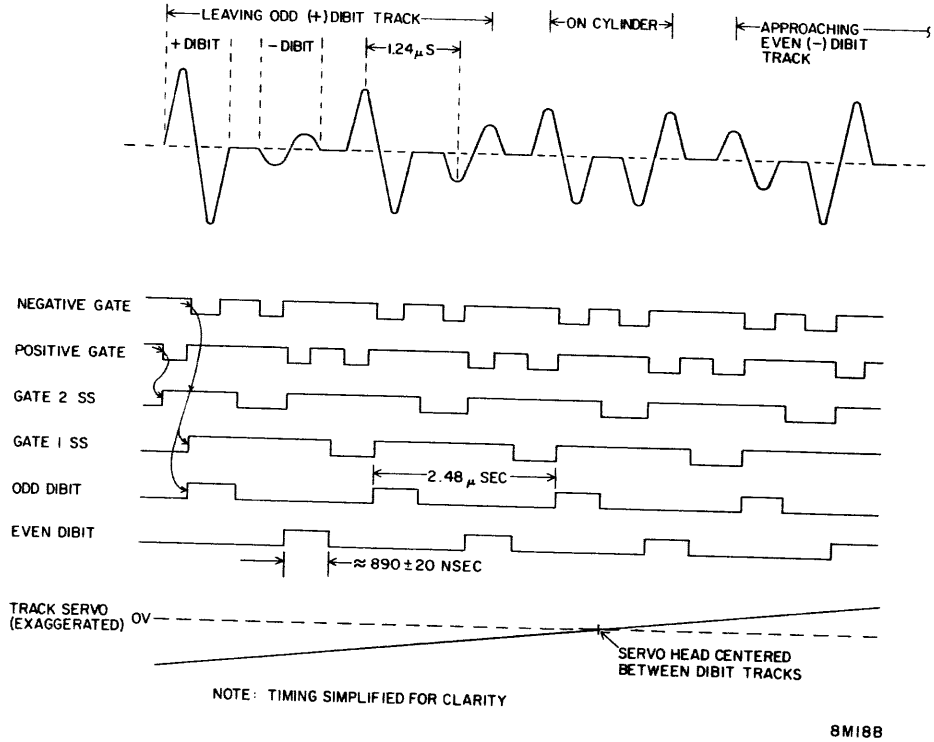


Figure 3-35. Track Servo Circuit - Signals and Timing

The servo signal is generated by the peak detectors that monitor their respective dibits. If the positive dibit amplitude exceeds the negative dibit amplitude, the output of the + dibits peak detector is greater than that of the - dibits pack detector. The outputs of these two detectors are applied to a summing amplifier whose output represents the distance between the two detector outputs. This output is the track servo signal. This signal is at its maximum negative value when the servo head is positioned over the outer guard band or over one of the odd dibit tracks. It is at its maximum positive value when the servo head is positioned over the inner guard band or over one of the even dibit tracks.

The track servo signal is applied to the servo circuit and to the cylinder detect circuit. In the servo circuit, it is used to generate the fine position analog signal that controls movement during the last one-half track of a seek or during a Load sequence. The cylinder detect circuit generates cylinder pulses as the track servo signal approaches a null.

Circuit gain control is achieved by applying the outputs from the peak detectors to a second summing amplifier. Its output is negative in proportion to signal strength: the stronger the signal, the less negative the agc voltage. This signal is applied to the agc amplifier to control the resistance of a FET within the amplifier. The FET is connected across the differential inputs to the amplifier. The less negative the agc, the less the resistance; therefore, more of the signal is shunted by the FET to reduce circuit gain.

Cylinder Pulse Generation

As the servo head crosses the interface of the even/odd dibit tracks (figure 3-36), the servo signal decreases toward null. The two detected cylinder pulses are ORed to a Schmitt trigger. The hysteresis designed into the trigger causes it to be up only while the servo signal is between 0v and 0.4v. This provides a 10 µsec cylinder pulse. Each cylinder pulse decrements the difference counter and switches the velocity integrator to ground.

It is possible that the last cylinder pulse may not be generated when the seek is completed, causing the difference counter to hang up at 001. The On Cylinder signal provides a pulse to decrease the difference counter to 000. With the difference counter at 000 (T=0) and On Cylinder available, the Seek Complete FF sets.

The track servo circuit remains active following completion of a seek. If the servo head drifts off of its centered position, the track servo signal will no longer be at null. The signal, functioning as the fine position analog signal within the servo circuit, will act as a position error signal to drive the positioner back into position.

CYLINDER CONCEPT

All heads are mounted and aligned vertically on the carriage (refer to figure 3-37). and when the carriage moves, all heads move together.

Therefore, when the servo head is positioned over a specific track on the servo surface, all other heads are positioned over the corresponding track on their respective disk surfaces. For example, if the servo head is over servo track 10, all other heads are also over track 10. This creates an imaginary cylinder as shown on figure 3-37.

PHYSICAL TO LOGICAL CYLINDER CORRELATION

The 150 MB and 300 MB drives both use the same disk pack. This pack has 823 cylinders that can be addressed and used for data recording.

These cylinders are numbered from 000 to 822 (refer to figure 3-38) and are defined as physical cylinders. Each track in these cylinders are defined as physical tracks.

A 300 MB drive is capable of addressing and seeking to 823 logical cylinder addresses (000 to 822). It therefore can seek to all 823 physical cylinders and the logical cylinder address corresponds to the physical address. For example, logical cylinder 000 is also physical cylinder 000 and logical cylinder 822 is also physical cylinder 822.

However, a 150 MB drive can address and is capable of seeking to only 411 logical cylinder addresses (000 - 410). For this reason, it seeks to only the even numbered physical cylinders. Therefore, logical cylinder 000 is physical cylinder 000 but logical cylinder 410 is physical cylinder 820.

The physical to logical track correlation for both the 150MB and 300MB units is shown on figure 3-38.

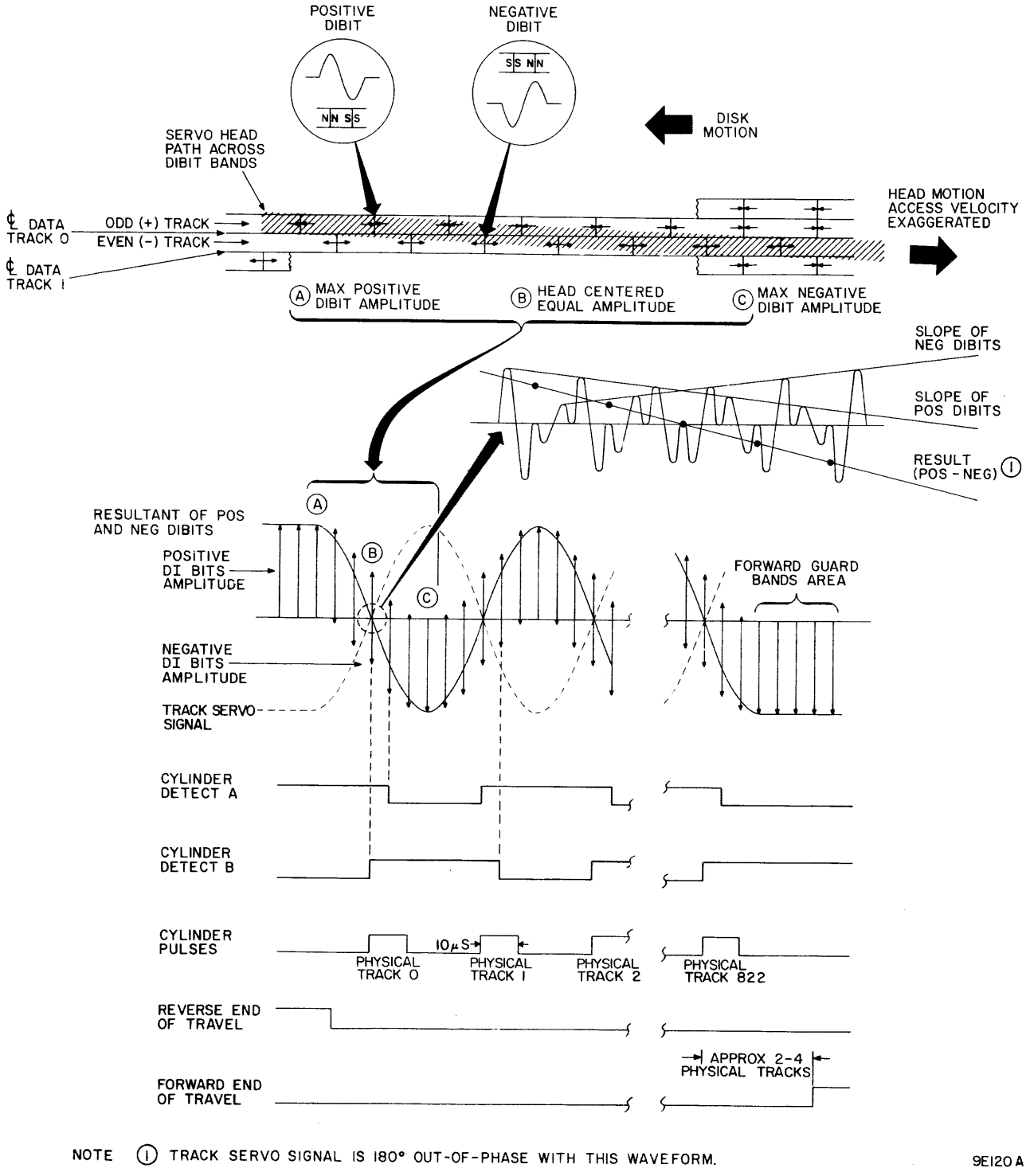


Figure 3-36. Cylinder Pulse Generation - Signals and Timing

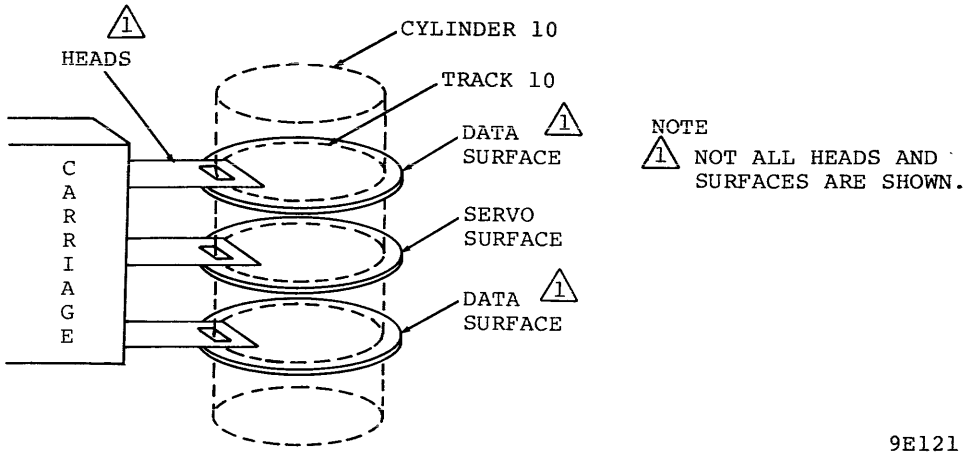


Figure 3-37. Cylinder Concept

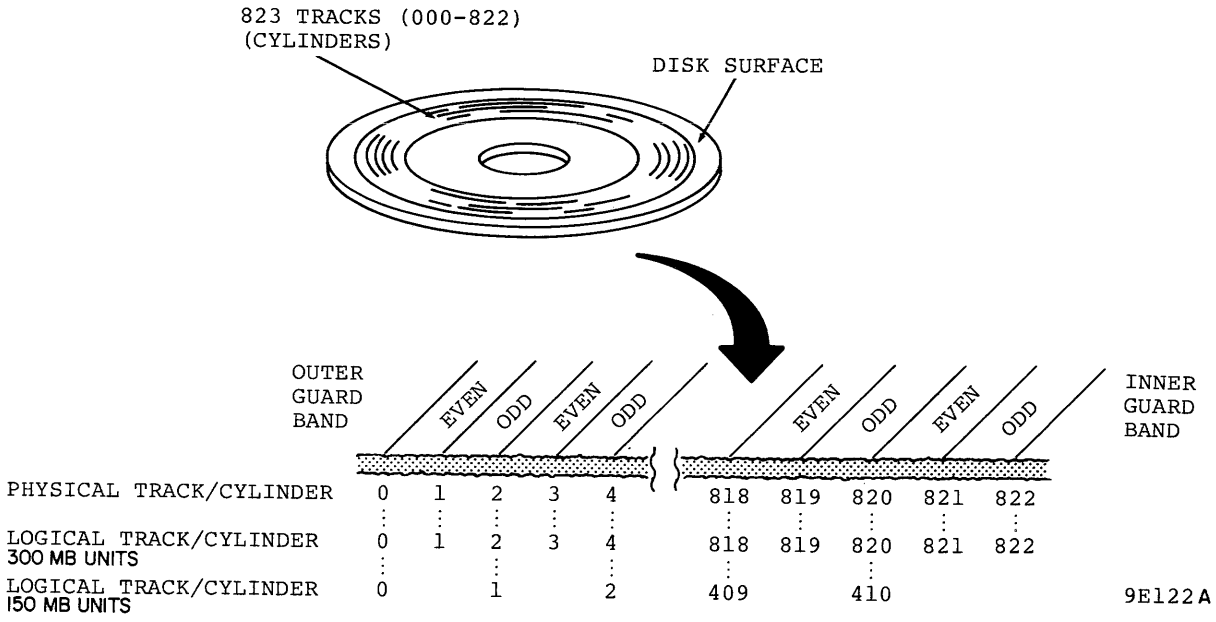


Figure 3-38. Physical to Logical Track Correlation

BASIC SEEK OPERATION

General

Seek operations are initiated by a series of control signals from the controller or by internally-generated signals within the drive during power up conditions. Most long seeks may be divided into four phases (see figure 3-39).

- Accelerate Phase: the voice coil receives full current to move the positioner from the current cylinder towards the new cylinder.
- Coast Phase: velocity is at its maximum and the positioner velocity is constant.
- Deceleration Phase: the positioner is approaching the desired cylinder. Its velocity must be reduced by braking action to prevent overshoot.
- Stop Phase: the positioner is almost at the desired cylinder. It must be stopped at the precise centerline of the new data cylinder. The logic is in Fine mode to stop and hold the positioner at the new cylinder.

Refer to the various seek descriptions for detailed information on the exact seek sequencing.

Acceleration Phase

This phase begins when the controller sends the desired address to the cylinder address register and adder. The adder combines the new address with the present address to obtain the difference. The difference is gated into the difference counter, which decrements until logical tracks-to-go equals zero.

The outputs of the difference counter are applied to the D/A converter. The value of these bits indicates the position error (or logical tracks-to-go) from 0 to 128 (64 on 150 MB units) that is, the amplitude of the D/A converter output is directly proportional to the number of tracks remaining in the seek. If the remaining seek length is greater than 128 (64 on 150 MB units), the D/A converter output is clamped at its maximum saturated value to cause the maximum error signal.

The input to the summing amplifier is now a large signal. Since there is no velocity yet, the current through the voice coil is maximum, causing maximum acceleration.

As the positioner accelerates, a velocity signal is generated by the velocity transducer. This signal opposes the position error signal. Its amplitude, however, is less. Acceleration continues.

Coast Phase

Eventually, the amplitude of the position error signal and the velocity feedback signal are equal. The net error signal in the loop drops to zero. The summing amplifier output follows, so current is cut off. Velocity is constant. Friction losses tend to slow the positioner but, as it does, the velocity signal decreases. This allows the position error signal to call for more current.

Deceleration Phase

Braking action starts as the positioner approaches its selected cylinder.

The track servo circuit (refer to Track Servo Circuit description) has been generating cylinder pulses as each physical cylinder passed. These pulses are used to decrement the difference counter.

When T≤128 (64 on 150 MB units), the D/A converter output steps down with each track crossed. This provides an output proportional to the number of tracks to go.

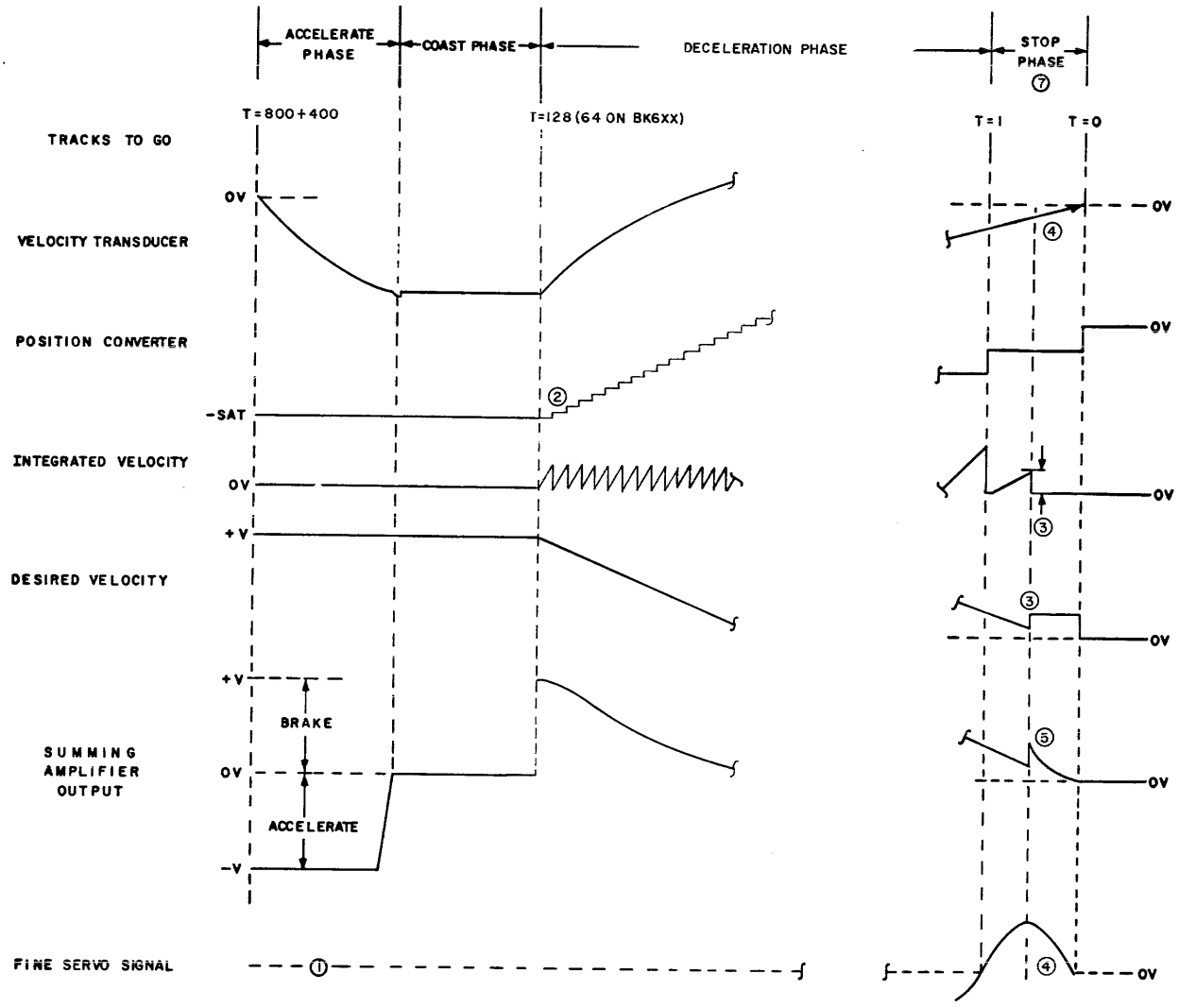
The D/A converter output is combined with the output of the Velocity Integrator.

The Velocity Integrator provides a sawtooth waveform the amplitude of which increases directly with velocity and time. The waveform is pulled back to zero by each cylinder pulse.

Combining the stepping down output of the D/A converter with the Integrated Velocity signal, results in a smooth curve of constantly decreasing magnitude.

This signal is then processed by the Desired Velocity Function Generator to produce the Desired Velocity signal. The Desired Velocity signal is then summed with the Velocity signal (output from the velocity transducer) and applied to the summing amplifier.

When the desired velocity signal becomes less than the Velocity signal, current is applied to the voice coil in the maximum reverse direction until the velocity of the carriage slows down below the instantaneous desired velocity value. The current to the voice coil is then lowered and the carriage coasts under its own inertia while the difference counter continues to count down (decreasing the



NOTES:

① SIGNAL HAS NO EFFECT UNTIL FINE LATCH SETS.

② OUTPUT DECREASES WITH EACH CYLINDER PULSE.

③ FINE LATCH SETS WHEN $T \leq 1$ AND INTEGRATED VELOCITY > 1.4V. DESIRED VELOCITY HAS NO FURTHER EFFECT.

④ COMBINATION OF THESE TWO SIGNALS CONTROLS OUTPUT FROM SUMMING AMPLIFIER.

⑤ GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. ALTHOUGH CONTINUOUS BRAKING ACTION IS ILLUSTRATED, OUTPUT MAY BE NEGATIVE (ACCELERATE) IF FINE SERVO SIGNAL EXCEEDS VELOCITY SIGNAL.

⑥ SCALE CHANGED AT T=1 FOR CLARITY.

⑦ DRAWING NOT TO SCALE FOR TIMING OR RELATIVE SIGNAL AMPLITUDE. IT IS SIMPLIFIED TO ILLUSTRATE SIGNAL FUNCTIONS.

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Figure 3-39. Servo Circuit Signals

desired velocity signal). If the carriage velocity becomes too high for the existing desired velocity signal, the current increases until the velocity slows down below the instantaneous desired velocity value.

Stop Phase

Stop Phase begins when the difference counter indicates that there is one logical track to go. When T=1, the velocity integrator signal is pulled back to zero by the cylinder pulse. Its output, indicating distance, increases. When its amplitude indicates approximately one-half track remains, Fine Enable sets the Fine Latch. Desired velocity is disabled since the coarse gate is opened by the Fine Latch being set.

The last half-track of motion is controlled by the Fine Position Analog signal which is derived from the Track Servo signal. Fine position and velocity are applied to the summing amplifier through the fine gate. The summing of these two signals controls the braking current.

At the start of the seek, the Slope FF is set if the seek is to an odd-numbered physical cylinder and cleared if it is to an even number physical cylinder. (Note that it is always clear on 150 MB units because all seeks are to even numbered physical cylinder.) The Slope signal controls the phase of the Fine Position Analog signal. This adjustment is required since Track Servo signal phasing is a function of the servo head position: the signal is positive when over negative dibits and negative when over positive dibits. Therefore, on forward seeks, the signal decreases when approaching a physical track with an odd number and increases when approaching a physical track with an even number. The opposite is true during a reverse seek.

The Fine Position Analog signal opposes the Velocity signal during the last half-track of the seek. Both signals are decreasing. If either is greater, the summing amplifier makes minor braking current adjustments. When the heads are on cylinder, both signals are zero and current is zero.

When the Fine Position Analog signal is less than about 0.3v the positioner is, for all practical purposes, positioned over the data track. This initiates the On Cylinder delay. After 1.75 ms, On Cylinder is returned to the controller.

The Fine Position Analog signal remains active even though On Cylinder is up. This is the track following or position error operation. Since the positioner is not mechanically locked in place, it can drift off cylinder. As long as it is precisely positioned, the dibits read from the adjacent dibit tracks are equal and opposite. Should the carriage move, one dibit signal will increase in amplitude. This results in a slight Track Servo signal which is translated into the Fine Position Analog signal. The summing amplifier, in turn, senses this off-null condition and drives the positioner back on cylinder.

If the positioner goes off cylinder sufficiently to cause a Fine Position Analog signal greater than 0.4v for more than 800 µsec, the On Cylinder signal is lost.

The loop also permits positioner offset if the program requires it for data recovery. A Seek Offset positive code provides a bias input to the fine position amplifier. This is now an error signal to the summing amplifier to cause a forward motion. This motion stops when the bias voltage and track servo voltage cancel. Seek Offset negative causes reverse offset. The offset is 250 µin for either a positive or a negative offset.

Short Seeks

The preceding explanation assumed that the seeks were long enough for the positioner to attain maximum velocity. Maximum velocity of about 65 ips requires approximately 250 tracks acceleration time. For shorter seeks maximum velocity is not achieved and the last phase does not exist.

During seeks less than 128 (64 on 150 MB units) tracks, the desired velocity signal is used immediately. This signal, with the actual velocity signal from the velocity transducer, generate an error voltage to control positioner movement. Acceleration occurs when the position error signal exceeds the velocity signal; braking occurs when the velocity signal exceeds the position error signal.

TYPES OF SEEKS

General

The drive performs 3 basic types of seeks:

- Load Seek - Initiated by pressing the START switch, it causes the heads to load and position themselves at logical cylinder 000.
- Direct (Forward/Reverse) Seek - Performed when the controller commands the drive to move the heads from one location to another.
- Return to Zero Seek - Initiated by the controller it causes the drive to position the heads at logical cylinder 000.

Load Seek

This function involves the activities that a unit must perform before it can effectively respond to a Read, Write, or Seek command from the controller. This function consists mainly of power supply relay sequencing and status checking by the units logic. As a result, no actual selection of the unit is required and very little drive/controller signal exchange occurs.

Successful progression of the function assumes that all circuit breakers are on, disk pack is installed on spindle of unit, and the interlock is closed. Successful completion of a load is signified by the occurrence of an On Cylinder and the lighting of the READY indicator.

Initiation of the function occurs when the operator panel START switch is pressed. See figure 3-40 for the load flow chart. The START switch initiates the power on sequence causing the drive motor to start rotating.

When the disk pack speed reaches approximately 2700 r/min, the power amplifier is connected to the voice coil. When one speed reaches 3000 r/min, the Load Latch sets. The Load latch activates circuitry to produce an average forward 7 ips access that mechanically loads the heads. The carriage continues forward with the servo head searching for the prerecorded positive dibit signals on the track servo surface. When the reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared, the Reverse EOT FF is set, and the Fine gate and latch are enabled. The carriage now moves under control of the Fine Position Analog signal. When even (negative) dibits are detected (approaching physical track 000) the Load latch and Reverse EOT FF clear. The carriage now decelerates.

The drive sends On Cylinder to the controller 1.75 ms after the Fine Position Analog signal is less than 0.3v. The carriage stops when the Fine Position Analog signal is 0v. The Servo Ready latch is then set, and the READY indicator is turned on. The drive is now ready to perform a Read, Write, or Seek operation.

If, for any reason, the dibit signals are not detected by the servo head within 350 ms after the Load latch is set, the RTZ latch is set and the carriage is retracted to the heads unloaded position. The FAULT indicator is then turned on. When the FAULT switch is pushed, the Fault latch is cleared and the carriage will attempt another seek to logical track 000. Once again if the dibit signals are not detected within 350 ms, the carriage will be retracted to the heads unloaded position and the FAULT indicator turned on.

Direct (Forward/Reverse) Seek

The Direct Seek funciton involves those operations that must be performed to move the read/write heads from their current logical track or cylinder location to the one specified by the controller. Refer to figures 3-41 and 3-42. Assume that the drive is at logical track 10 and awaiting further instructions. Assume also that the controller wishes to do a Read or Write operation at track 320. When the controller determines that the drive is ready, it sends the new cylinder address along with Tag 1. Raising Tag 1 places the old address and compliment of the new address in the adder. After the compare has been made, the difference counter is loaded with the number of tracks to go. When the controller drops Tag 1, the new cylinder address is loaded into the CAR, the seek direction is sent to the servo, and a Start Seek pulse is generated. (Refer to the servo circuit discussion for general seek functions.)

The Forward Seek signal from the cylinder address adder gates the output of the D/A converter (Position Error signal) into the desired velocity function generator. (A Reverse Seek would have gated an inverted Position Error signal.) Since the seek length is greater than 128 (64 on 150 MB units) logical tracks, the D/A converter output is clamped at maximum voltage. Set Seek clears the Fine latch, so the output of the Desired Velocity signal is gated through the coarse gate to the summing amplifier. Since the carriage is stationary, no Velocity signal exists to balance the Position Error, and forward motion of the carriage begins.

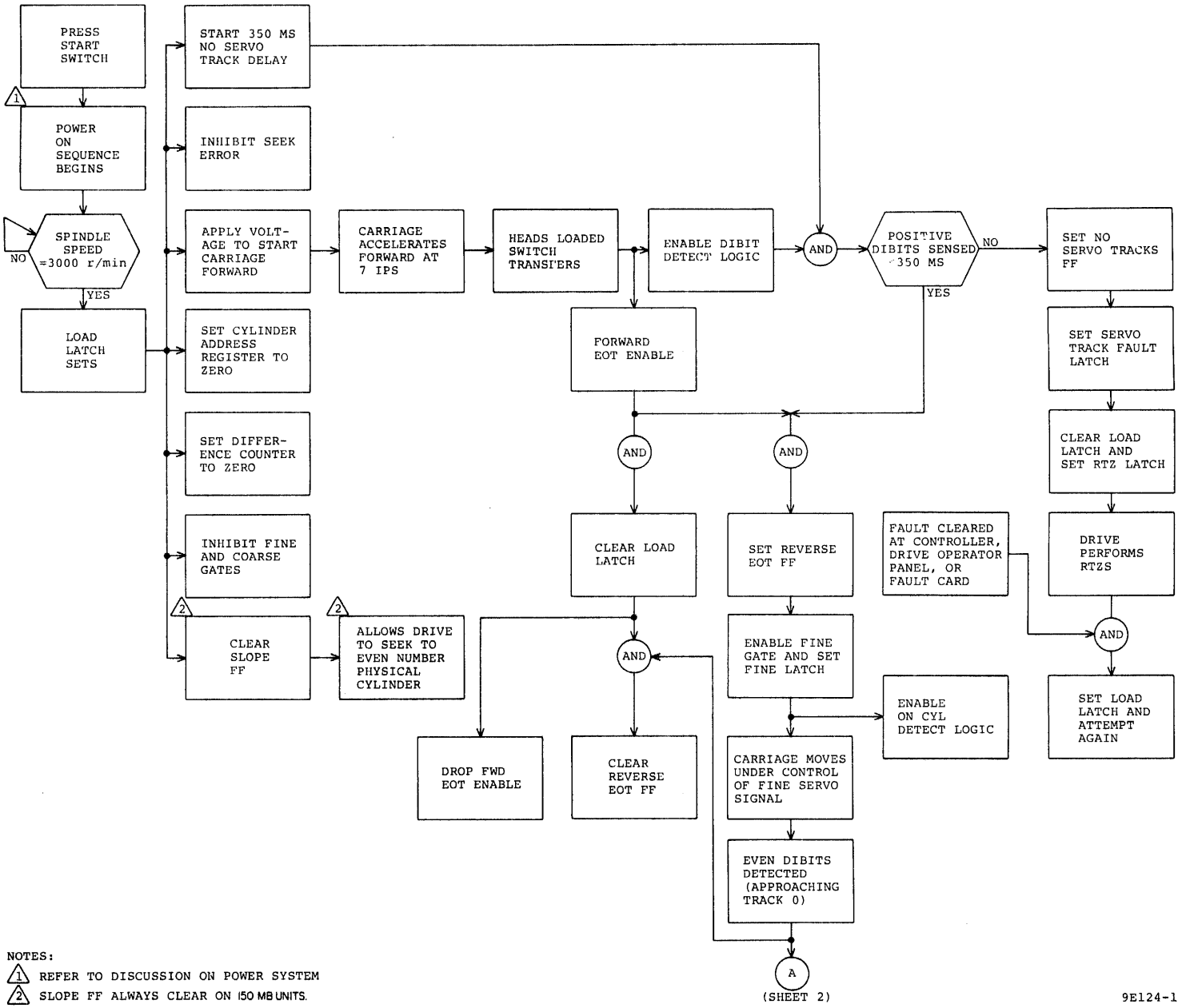


Figure 3-40. Load Seek Flow Chart (Sheet 1 of 2)

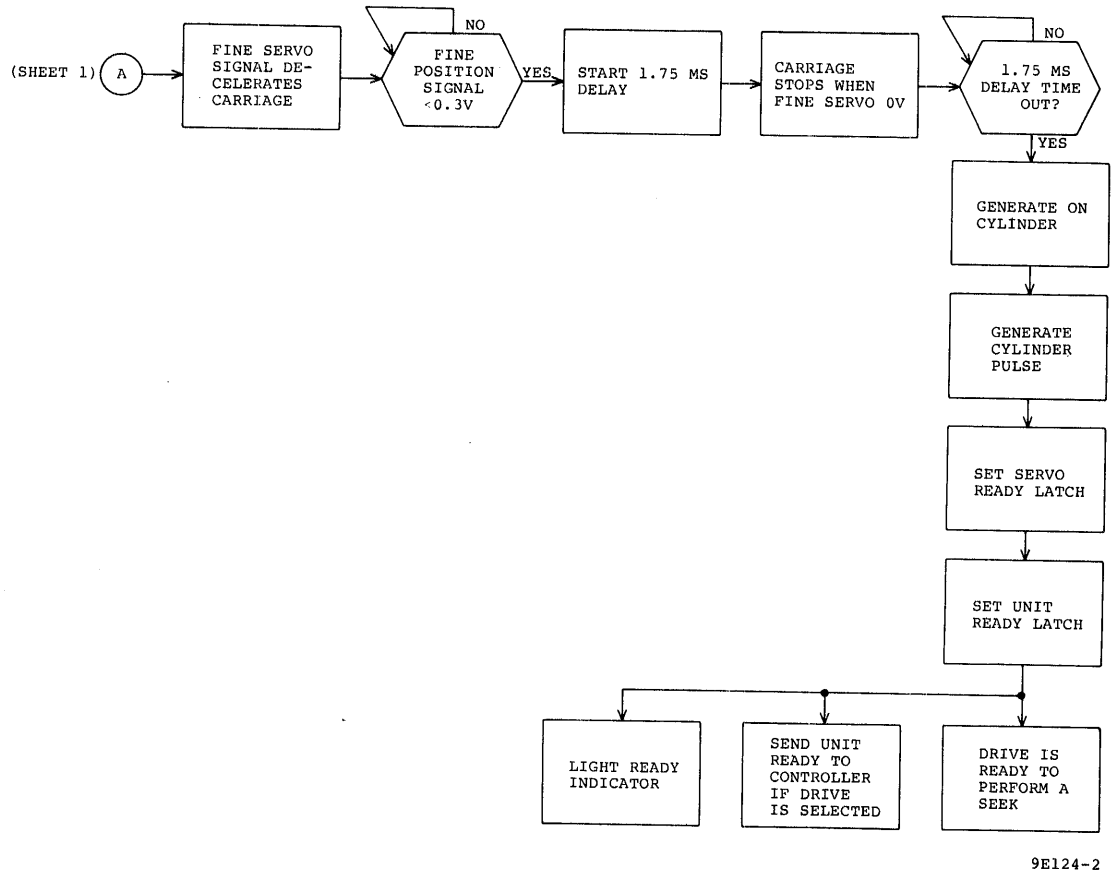


Figure 3-40. Load Seek Flow Chart (Sheet 2 of 2)

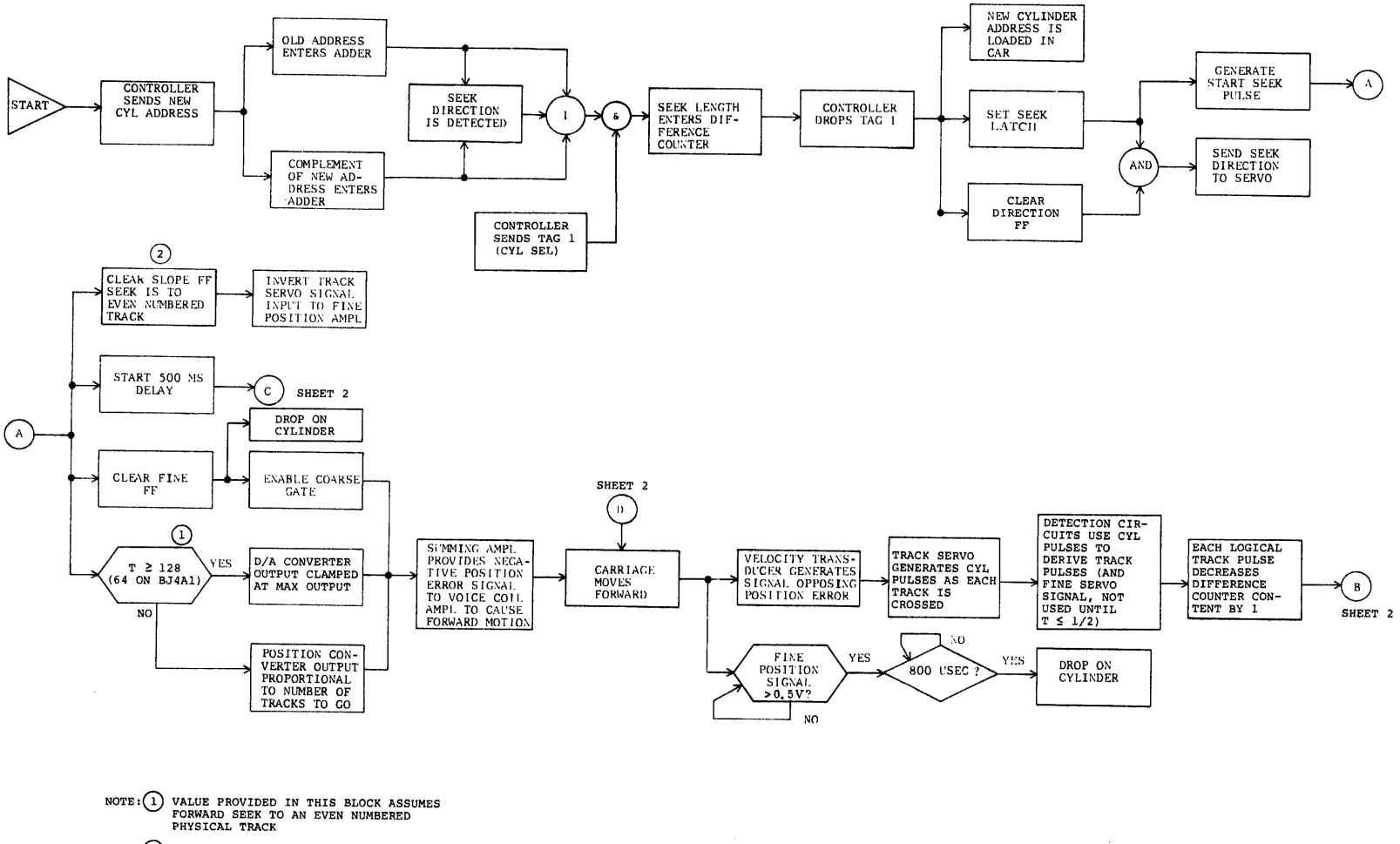


Figure 3-41. Direct Seek Flow Chart (Sheet 1 of 2)

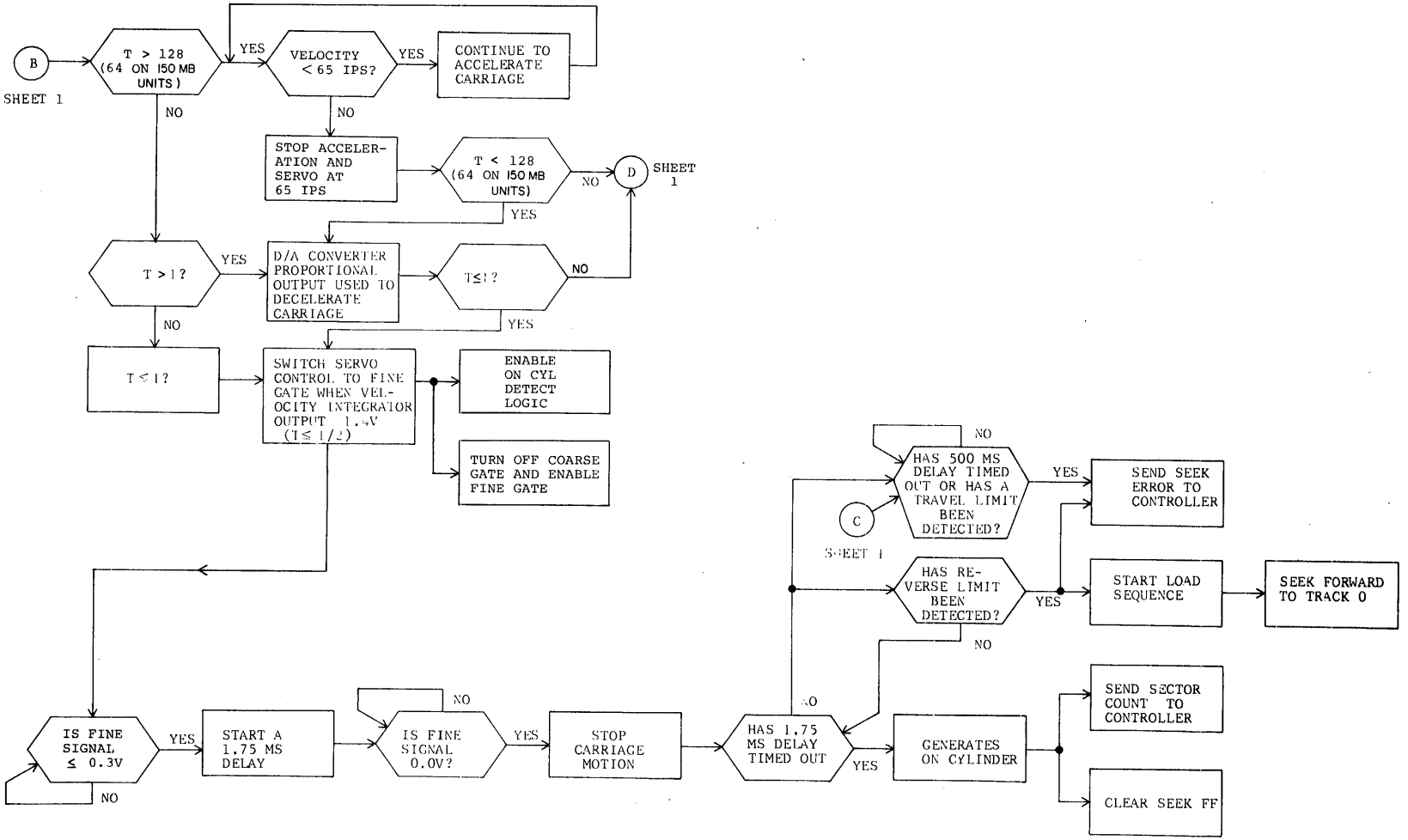
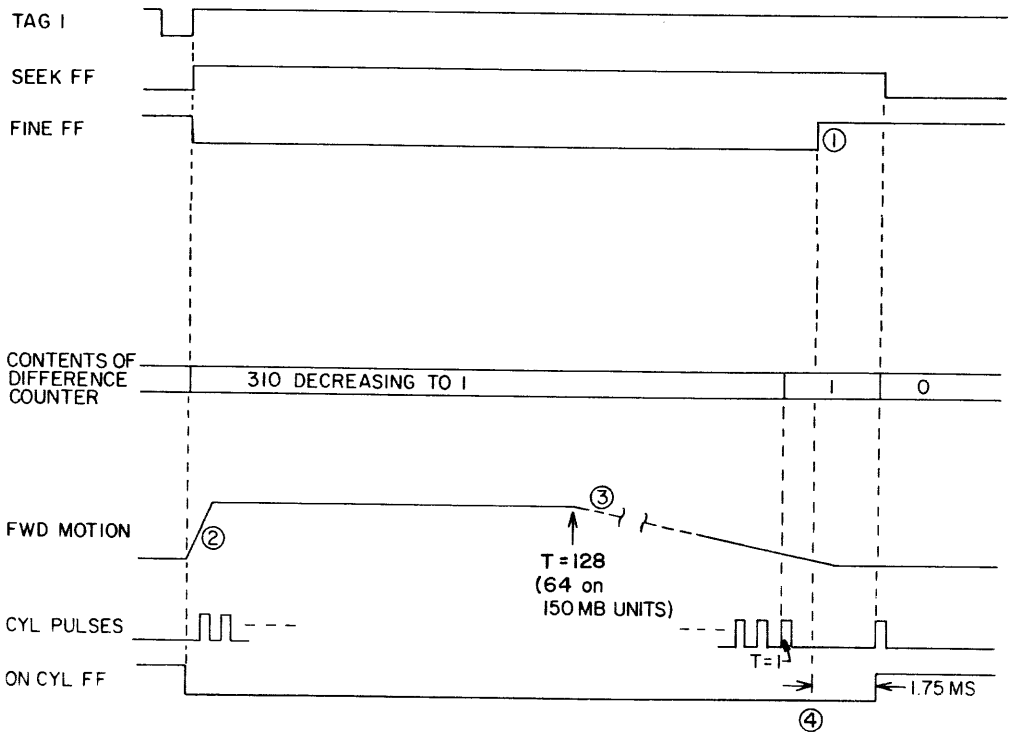


Figure 3-41. Direct Seek Flow Chart (Sheet 2 of 2)



NOTES: ① FINE FF SETS WHEN VELOCITY INTEGRATOR OUTPUT ≤ 1.4V AND T ≤ 1.
② APPROXIMATELY 250 TRACKS REQUIRED TO ACCELERATE TO 65 IPS.
③ CARRIAGE DECELERATES.
④ ON CYLINDER DELAY STARTS WHEN FINE POSITION SIGNAL<0.3V.
⑤ TIMES ARE NOT TO SCALE.

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Figure 3-42. Direct Seek Timing

With the Position Error signal clamped at maximum, the power amplifier output (and voice coil positioner current) will be maximum and the carriage will continue to accelerate. As the carriage moves forward, outputs from the track servo head are processed to derive a cylinder pulse as each cylinder is crossed. Each pulse (every other pulse on 150 MB units) decreases the content of the difference counter by one. When acceleration has increased to the point where the Velocity Amplifier signal and the Position Error signal cancel each other, the Summing Amplifier Control signal drops off. During this phase, the carriage coasts along the 65 ips plateau with the power amplifier providing only enough output voltage to compensate for the back emf of the moving voice coil positioner.

When the tracks remaining in the Seek are 128 (64 on 150 MB units), the DA converter voltage clamp is disabled, and for the remainder of the Seek (except for the last logical track), the servo position error is derived from the D/A converter. As each track is crossed, the D/A converter output steps down by a precise and linear amount. So that the position error provided at the desired velocity function generator input is not stepped, the integrator clamp gates the velocity integrator on between each cylinder pulse. The resulting integrator sawtooth output is added to the D/A converter output and fills-in the area between the leading edges of each step.

When the position error signal becomes less than the Velocity signal, current is applied to the voice coil in the maximum reverse direction until the velocity of the carriage slows down below the instantaneous position error value. The current to the voice coil is then turned off and the carriage coasts under its own inertia while the difference counter continues to count down (decreasing the position error signal). If the carriage velocity becomes too high for existing position error signal, a maximum reverse current is again applied until the velocity slows down below the instantaneous position error value.

When the counter indicates one track to go the desired destination, the Integrated Velocity signal is reset by the regular cylinder pulse. The Integrated Velocity, which indicates distance, brings up Fine Enable when the one-half track of travel remains. This sets the Fine latch which, in turn, enables the Fine gate and disables the Coarse gate.

Desired velocity no longer has an effect; the position error is supplied by the Fine Position Analog signal. This signal is derived from the Track Servo signal from the track servo circuit. The amplitude of the signal is proportional to the distance between current head position and the desired logical cylinder.

Since the desired destination is logical track 320, bit 0 of the Address register is "0". This causes the Slope FF to be cleared (note that it is always clear on 150 MB units). As a result, the Track Servo signal is inverted to form the Fine Position Analog signal. In all seeks, the Fine Position Analog signal is phased to be opposite to the Velocity signal. As the carriage approaches logical track 320, the Fine Position Analog signal approaches 0v. The summing amplifier responds to this decrease in amplitude by decelerating the carriage so that the sum of the Velocity signal always just cancels the Fine Position Analog signal. At track 320, both Velocity and position error equal zero, and all motion stops with the servo circuit at null. Only a position error will cause additional motion. When the Fine Position Analog signal is less than 0.3v, a delay of 1.75 ms starts. The On Cylinder signal occurs when the delay times out.

Certain conditions indicate that the seek was not completed successfully. This is a Seek Error. These conditions are:

- On Cylinder not generated within 500 ms from the start of the seek.
- Forward EOT sensed. The carriage returns to logical cylinder 822 (410 on 150 MB units) and remains there.
- Reverse EOT sensed. The carriage returns to logical cylinder 000 and remains there.
- If the carriage drifts off cylinder enough for the fine position signal to be greater than about 1.61 volt for more than 800 µsec, the Seek Error FF sets. In addition, if the drive is reading or writing, the Fault FF also sets. Write gate is disabled. The unit will not accept any commands until the error is cleared manually.
- Command seek to track greater than 822 (410 on 150 MB units).

All of these conditions require an RTZ command to clear the error. RTZ clears Seek Error and returns the drive to logical cylinder 000.

Reverse seeks function in an identical manner, except that all phases and polarities are reversed. Total seek times for forward or reverse seeks are identical for seeks of equivalent lengths.

Return to Zero Seek (RTZS)

The RTZ function allows a controller to return the heads to logical track 000 when a Seek Error occurs. See figures 3-43 and 3-44 for the RTZs flow chart and timing diagrams.

The RTZs pulse sets the RTZ latch and clears the Seek Error FF. This enables the RTZ gate, resulting in a bias voltage that forces an average 7 ips reverse motion of the carriage. When the carriage passes physical cylinder 000, no more even dibits are deteted. This is the Reverse EOT area. The loss of even dibits inhibits cylinder pulses, allowing the velocity integrator in the track servo circuit to reach a negative output in excess of 1.4v. This, along with odd dibits, sets the Reverse EOT FF. The integrator is reset, but reverse motion continues unimpeded.

After an additional reverse motion of about two to four tracks, the velocity integrator output again exceeds 1.4v. The RTZ latch is cleared while the Load latch sets.

The Load latch activates circuitry to produce an average forward 7 ips access. The carriage continues forward with the servo head searching for the prerecorded positive dibit signals on the track servo surface. When the reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared, the Reverse EOT FF is set, and the Fine gate and latch are enabled. The carriage now moves under control of the Fine Position analog signal. When even dibits are detected (approaching physical track 000), this signal decelerates the carriage.

The drive sends On Cylinder to the controller 1.75 ms after the Fine Position signal is less 0.3v. The carriage stops when the signal is 0v. The sequence must be completed within 500 ms after RTZs initiation, or else the Seek Error FF is set.

The RTZs function is also used during normal power off sequencing. If the START switch is pressed by the operator, the control interlock opens. This raises the Unload Heads signal in the drive logic. The RTZ latch sets to initiate a 7 ips reverse seek.

This time, however, the EOT Enable circuit is disabled so that the velocity integrator signal has no effect. In turn, the Load latch is disabled. Reverse motion continues until the heads unload.

The RTZs function transfers automatically to the heads unloaded condition if dibits are lost for more than 350 ms.

END OF TRAVEL DETECTION

The end of travel circuit determines when the heads are positioned outside of the normal data cylinders. This function is used during Load and RTZ sequences and to indicate an error condition during a seek.

Forward EOT indicates that the heads are within the inner guard band. Assume that the controller has commanded a forward seek and the positioner proceeds past cylinder 822 (410 on 150 MB units). Sequencing is as follows:

1. As the heads move forward, the velocity integrator output produces a signal proportional to velocity (the input to the integrator) and time (provided by the integrator capacitor). The input, which is a positive-going ramp during forward seeks, represents distance travelled. It is pulled back to ground by cylinder pulses. As long as cylinder pulses are generated, the output cannot reach an effective value.

2. After track 822 (410 on 150 MB units) is passed, no more odd dibit tracks are detected, resulting in no more cylinder pulses to reset the velocity integrator. When the output exceeds approximately 1.4v (2 tracks), Forward EOT Enable comes up. This signal, in conjunction with the even dibits picked off of the inner guard bank, sets the Forward EOT FF.

   With the Forward EOT FF set:

   a. Seek Error FF sets to return Seek Error to the controller.

   b. Seek FF (set at the start of the seek) is cleared.

   c. The difference counter is set to 000 (T=0).

   d. Fine Enable is raised within the servo circuit.

   e. Because of c and d, the Fine Gate in the servo circuit is enabled.

   f. The Slope FF is cleared to indicate a seek to an even-numbered cylinder (Note that it is always clear on 150 MB units).

3. The track servo, functioning as the Fine Position Analog signal in the servo circuit, is gated to the servo summing amplifier via the Fine Gate. The signal is at a maximum amplitude

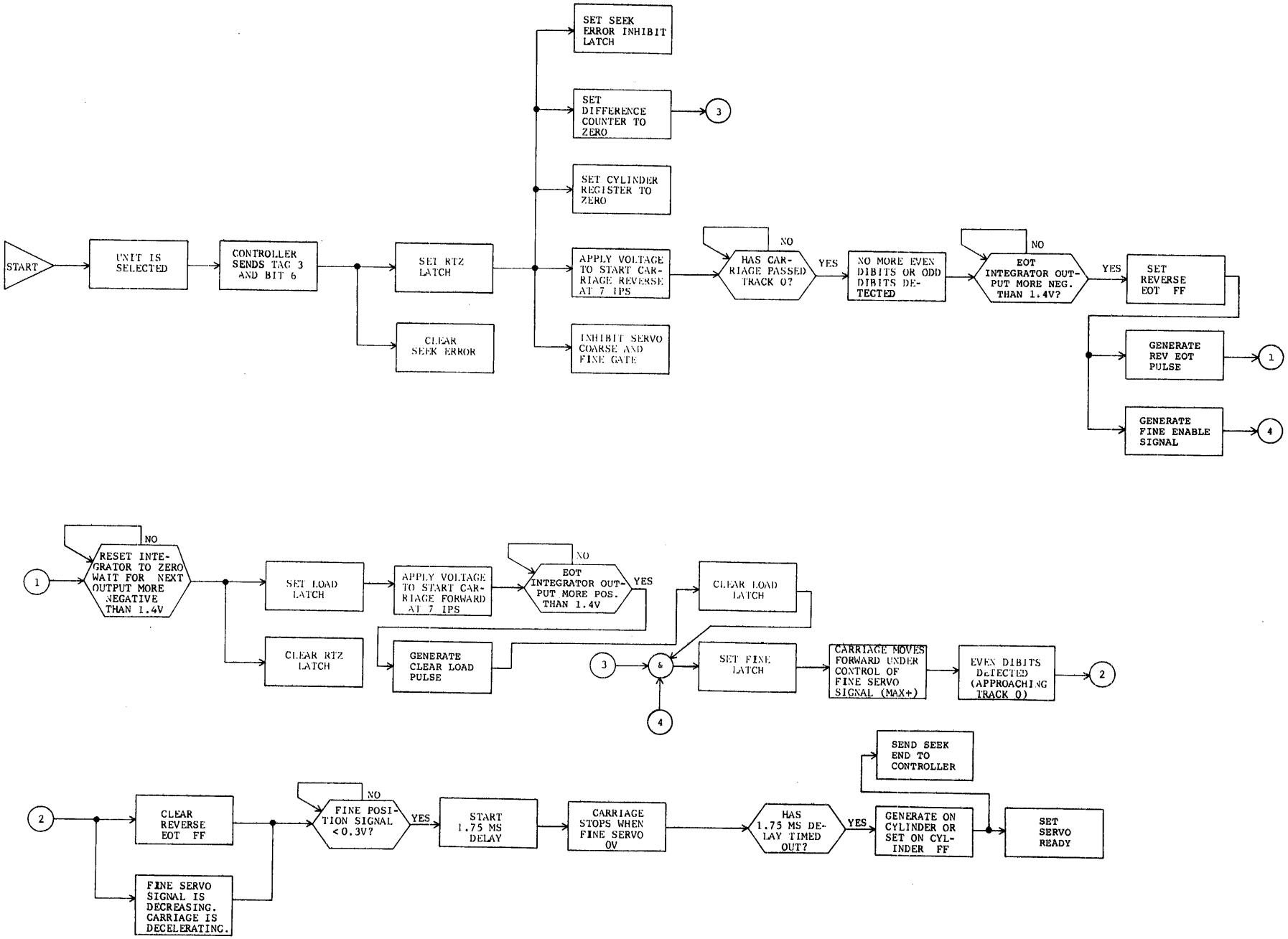

Figure 3-43. Return to Zero Seek Flow Chart

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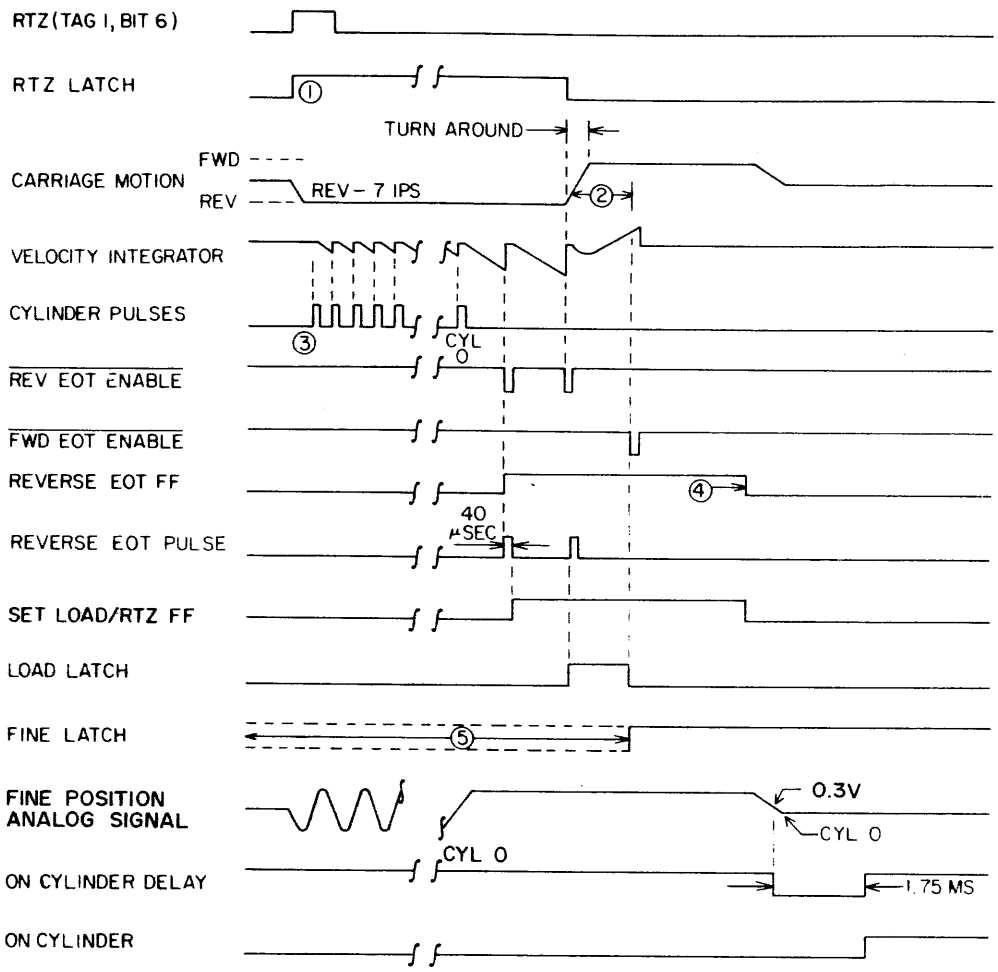

NOTES:

① RTZ LATCH CAUSES RTZ GATE TO APPLY NEG VOLTAGE (SEEK REV) TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO ZERO.

② FWD MOTION TO 7 IPS PROVIDED BY LOAD GATE, IT PROVIDES + (SEEK FWD) TO SUMMING AMPL. WHEN LOAD LATCH CLEARS, MOTION CONTROL PROVIDED BY FINE SERVO SIGNAL.

③ CYLINDER PULSES RESTART VELOCITY INTEGRATOR. THEY DO NOT AFFECT DIFFERENCE COUNTER.

④ REVERSE EOT FF CLEARED BY FIRST EVEN DI BITS. (APPROACHING TRACK 0).

⑤ BOTH OUTPUTS ARE HIGH WITH EITHER RTZ OR LOAD LATCH SET. THIS DISABLES COARSE AND FINE GATES. FF THEN SET BY T ≤ I AND FINE ENABLE.

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Figure 3-44. Return To Zero Seek Timing

because only even dibits are being sensed. This error voltage causes the positioner to drive in reverse until the servo signal drops to zero; the heads are then positioned at cylinder 822 (410 on 150 MB units).

4. An RTZ command is required to clear the Seek Error status.

Reverse EOT indicates that the heads are positioned over the outer guard band. If this condition occurs during regular reverse seeks, the Reverse EOT FF sets. This initiates an automatic Load sequence to return the actuator to logical cylinder 000.

MACHINE CLOCK

GENERAL

The machine clock circuits generate the clock signals necessary for drive operation. These circuits are divided into two areas (1) Servo Clock Multiplier and (2) Write Clock Multiplier. These are both explained in the following discussions.

SERVO CLOCK MULTIPLIER

The servo clock multiplier circuits generate clock pulses used by the sector detection, Index detection and the Read PLO circuits. It also generates the 9.67 MHz Servo Clock signal that is sent to the controller.

The main element in the servo clock multiplier circuit is the phase lock loop. This loop consists of a phase and frequency detector, error amplifier, voltage controlled oscillator and a divide by 12 circuit. The function of the loop is to adjust itself until its output is identical in phase and frequency to its input.

The input to the loop consists of the dibit signals from the track servo circuit. The nominal frequency of these signals is 806 kHz; however, their actual frequency is a function of and varies directly with disk pack speed. This means that the output of the loop will also vary with disk pack speed.

The phase and frequency detection circuit makes the comparison between the input dibits and the output of the loop.

The input dibits are applied via two retriggerable multi-vibrators. One of these multivibrators provides a 750 ns (approximate) output pulse which is then fed through a pulse forming circuit to provide a 25 ns input pulse for the phase and frequency detector. These pulses vary at the dibit frequency. The other multivibrator has a 1.6 µs output which is used to enable the feedback pulses from the loop output to the input of the phase and frequency detector. The 1.6 µs pulse is longer than the period of the nominal dibit frequency (806 KHz); therefore, the feedback pulses are continuously gated as long as dibits are present.

The outputs from the detector are fixed amplitude pulses which are a function of the time (or phase) difference between the positive going edges of the two inputs (refer to figure 3-45).

These outputs are applied to the error amplifier which integrates them and generates a voltage proportional to the phase difference between them. This voltage is used as a control voltage for the Voltage controlled oscillator.

The control voltage causes the VCO frequency to vary in the direction necessary to eliminate the phase or frequency difference between the input and output of the loop. The VCO output is then divided by 12, by the divide by 12 circuit, and fed back to the loop input.

When the VCO output is 9.67 MHz, the feedback provided by the divide by 12 circuit will be 806 KHz and the loop will be synchronized.

Both the 9.67 MHz and 806 KHz signals are divided by two thus producing 4.84 MHz and 403 KHz signals. All four of these frequencies are used by the drive as shown on figure 3-45.

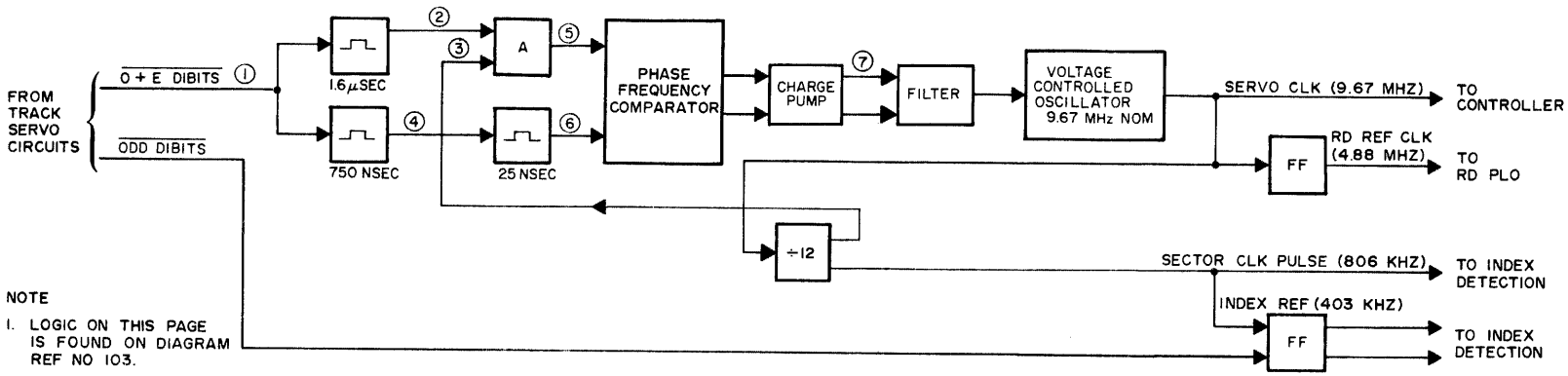
WRITE CLOCK FREQUENCY MULTIPLIER

The write clock frequency multiplier circuit (refer to figure 3-46) generates the 19.34 MHz and 9.67 kHz signals used during write operations.

This circuit consists mainly of a phase lock loop and operates essentially the same as the servo clock multiplier. However, the input to the write clock multiplier is the 9.67 MHz Write Clock signals from the controller. The phase lock loop synchronizes to these signals and provides the 19.34 MHz and 9.67 MHz outputs. These outputs are used by the NRZ to MFM converter and Write Compensation circuits during write operations.

INDEX DETECTION

Each track on the servo disk contains a pattern of missing dibits referred to as the Index pattern. When the drives Index Detection circuits (refer to figure 3-45) detect this pattern, they generate a 2.5 µs Index signal. The Index signal indicates, both to the drive and controller, the logic beginning of a track.



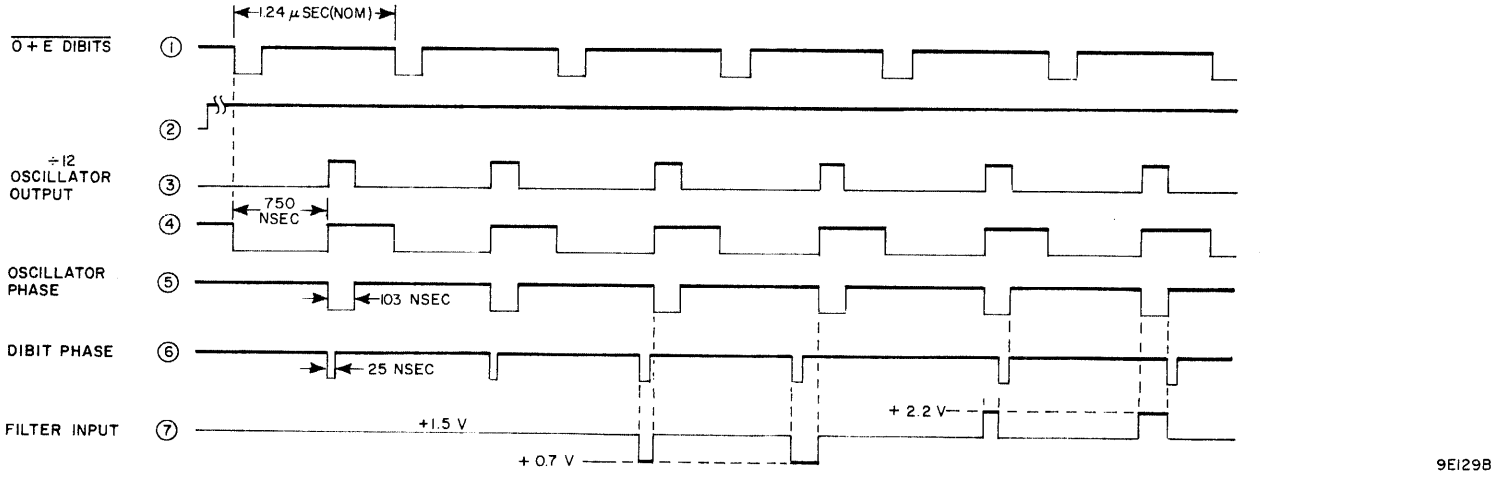
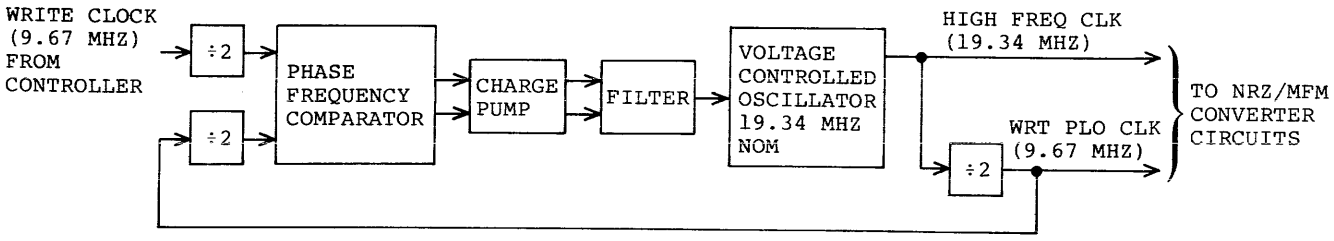


Figure 3-45. Servo Clock Multiplier



NOTE
1. LOGIC ON THIS PAGE IS FOUND ON DIAGRAM REF. NUMBER 104.

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Figure 3-46. Write Clock Multiplier

The Odd Or Even Dibits signal provides the data necessary to actually detect the missing dibit pattern. This signal is derived from the dibits detected from the disk and has a nominal frequency of 806 KHz. Because this signal is derived from the dibits, whenever a dibit is missing an Odd or Even Dibits pulse is also missing.

Detection of missing dibits is done by the Missing Dibits one shot. This one shot is triggered by the Odd Or Even Dibits signals and will not time out as long as dibits are present. However, if two or more consecutive dibits are missed the one shot times out. The output of the Missing Dibits one shot provides the data input for the first stage of the Index Shift register.

The Index Shift register loads the output of the missing Dibits one shot into its first stage (and also performs its shift) each time a 403 KHz Index Reference Clock pulse occurs. When the one shot is in a triggered state (indicating dibits were present) a one is present) a one is loaded into the register. However, when the one shot is timed out (indicating two or more dibits were missing) a zero loads into the register.

The contents of the Index shift register are continuously compared to the Index pattern by the Index Decoder and when the shift register contains the pattern indicating Index has occurred, the Index Decoder generates an Index signal. The missing dibit pattern associated with Index and the pattern contained in the shift register when Index has occurred are shown on figure 3-45.

In summary, the Index detection circuit contains three main elements:

- Missing Dibits one shot - Detects the missing dibits in the Index pattern.
- Index Shift register - Accumulates the dibit pattern so that it can be compared with the pattern occurring during Index.
- Index Decoder - Compares the contents of the Index Shift register with the Index pattern and generates an output signal when Index is detected.

These elements work in conjunction with the two input signals (Odd Or Even Dibits and 403 KHz Index Reference Clock) to produce the Index signal. The Index signal is sent to the controller and is also used to reset the drives sector detection circuitry.

SECTOR DETECTION

The sector detection circuits (refer to figure 3-48) generate signals which are used by the system to determine the angular position of the heads with respect to Index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disk pack. The Sector pulses logically divide the disk into areas called sectors.

The Sector pulses are generated by the Sector counter which causes a pulse to be generated each time it indicates its maximum value of 4095.

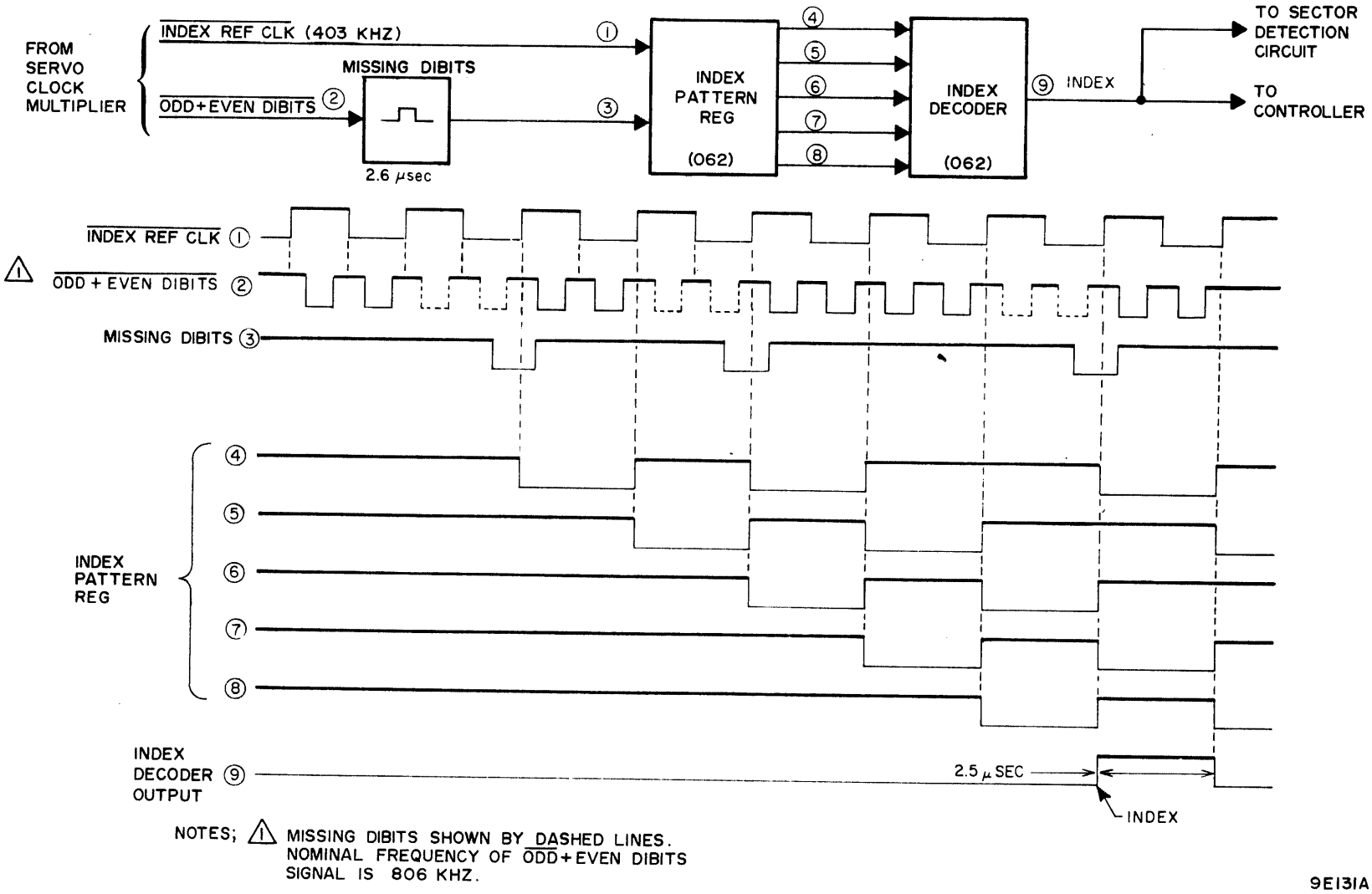


Figure 3-47. Index Detection - Logic and Timing

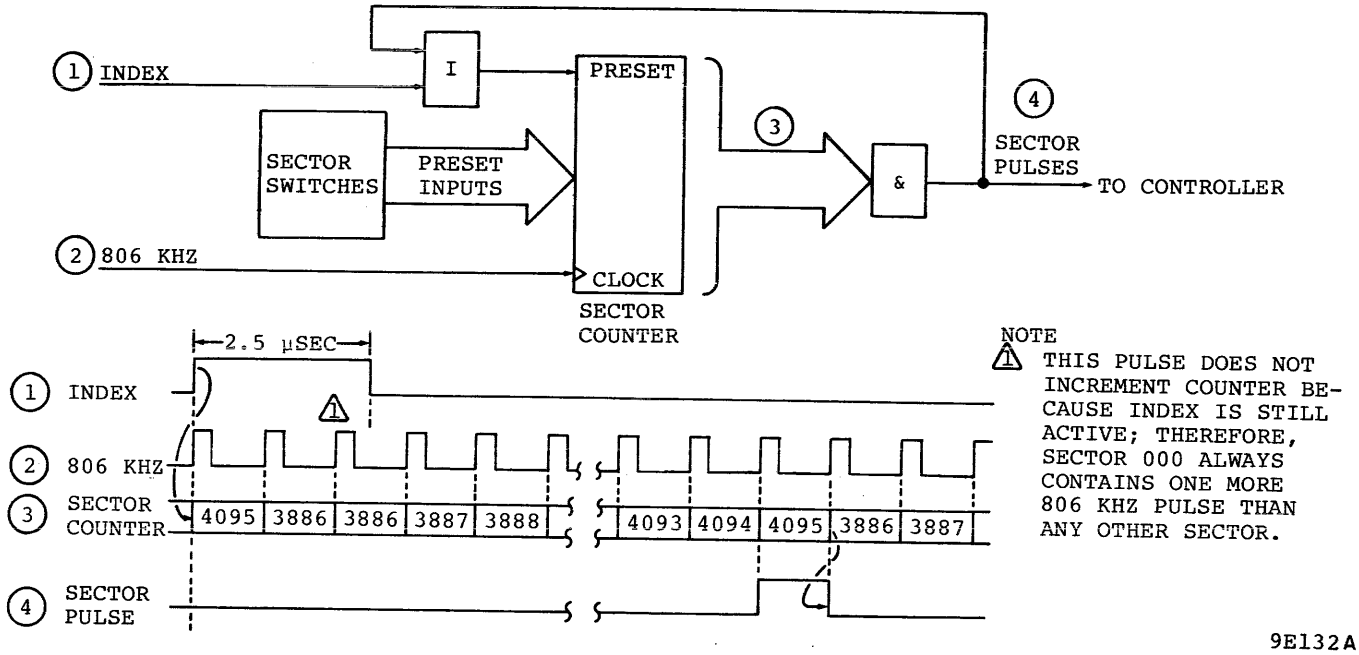


Figure 3-48. Sector Detection - Logic and Timing

The Sector counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the servo track dibit signals (refer to discussion on track servo circuit) and exactly 13,440 clock pulses occur during each revolution of the disk pack.

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sector (13,440 divided by 64) and the counter would be preset to 3786. In this case the counter starts at 3886 and increments each clock time until it reaches the maximum count of 4095. Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector. The 3886 is obtained by subtracting 210 from 4096, which is the total number of clock pulses the counter is capable of counting (0 through 4095 = 4096).

The sector length is varied by changing the value of the preset inputs to the counter. This is done by resetting the sector switches located on the card in logic chassis position A06. Refer to section 1 of the maintenance manual for details regarding the setting of the sector switches.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Head selection starts when the controller sends the drive a Head Select tag (2) and a head address. The head address is sent on Bus Bits 0 through 4.

The Head Select tag gates the address into the Head Address register. This address is then decoded to a Head Enable signal (0 through 18 depending on Bus O Bits 0 through 4). This signal then enables the head current driver associated with the addressed head and allows the head to conduct as shown on figure 3-49.

If more than one head is selected, a fault is indicated (refer to discussion on Fault and Error Conditions).

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending the drive a Control tag (3) and the proper bus bits (refer to discussion on Interface function).

During a read operation, the drive recovers data from the disk and transfers it to the controller. During a write operation, the drive receives data from the controller and records it on the disk.

Figure 3-50 is a block diagram of the read/write circuits. The remainder of this discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles - Explains the basic principles of recording data on and recovering data from a magnetic disk.
- Read Circuits - Describes the circuits used by the drive to recover data from the disk.
- Write Circuits - Describes the circuits used by the drive to record data on the disk.

BASIC READ/WRITE PRINCIPLES

General

Information is recorded on and read from the disk by the read/write heads. The following discusses the physical principles involved and techniques used in this process.

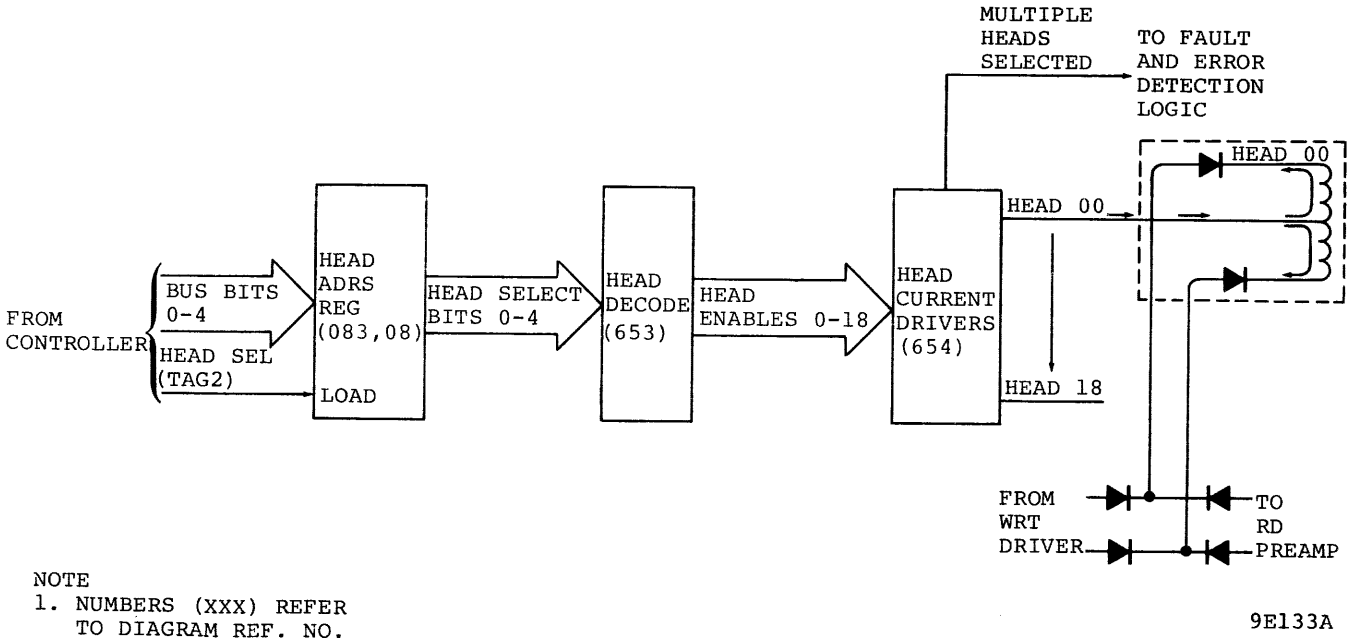


Figure 3-49. Head Select Circuits

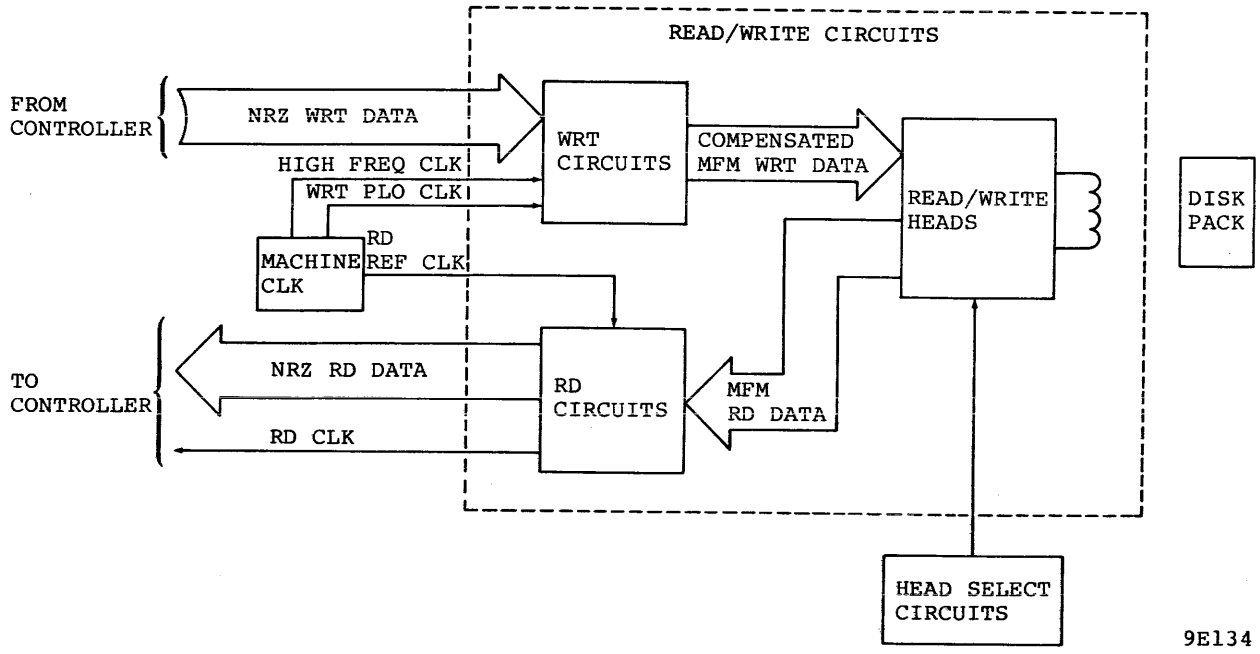


Figure 3-50. Read/Write Circuits Block Diagram

Writing Data On Disk

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (figure 3-51). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already be on the disk. The write current is zoned in eight current zones to ensure proper saturation level for best head resolution. The write current is maximum on the outer tracks and progressively decreased for inner tracks.

Reading Data From Disk

As the disk passes beneath the read/write head, the stored flux intersects the gap (figure 3-52). Gap motion through the flux induces a voltage in the head windings. This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

Peak Shift

Peak shift is an effect that degrades read accuracy by distorting the waveform. This condition exists because no electromechanical device can be perfect.

Ideally, the flux reversal command by the write toggle would be instantaneous as shown in the Ideal Recording portion of figure 3-53. Current would immediately switch from one polarity to the other. As a result, the distance required to complete the magnetic flux reversal on the disk would be so narrow as to be insignificant; the readback pulse would then also be extremely narrow. To carry the principle

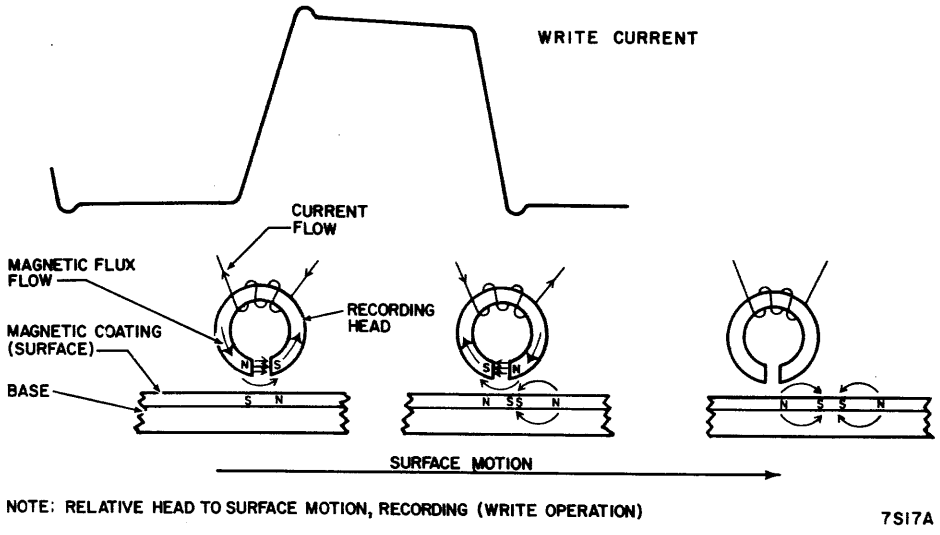


Figure 3-51. Writing Data

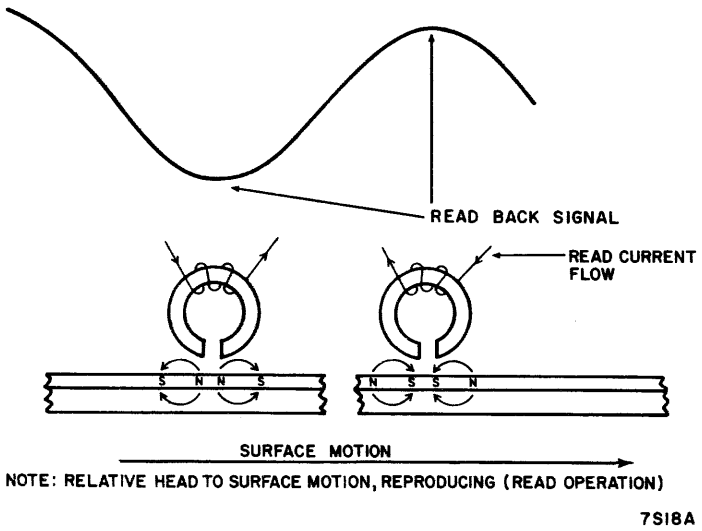


Figure 3-52. Reading Data

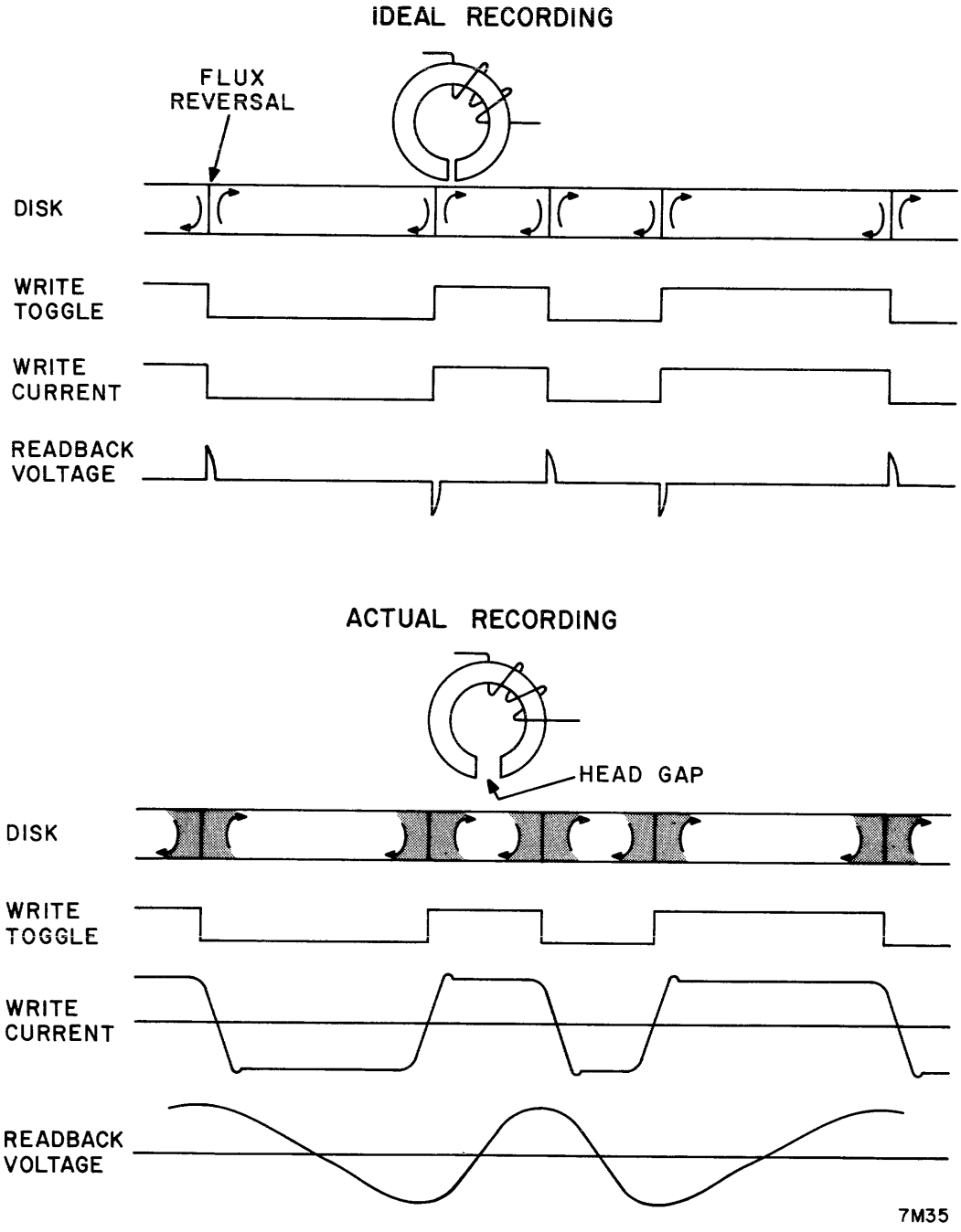


Figure 3-53. Write Irregularity - Typical Waveforms and Timing

one step further, the heads would be an infinitesimal distance from the disk surface. Therefore, the head gap itself could be made very small for two reasons:

- The magnetic field strength increases as the head moves closer to the disk.
- The head gap must be wide enough to intersect sufficient lines of force from the magnetic flux field to generate a signal. The weaker the signal, the wider the gap must be. With the substantial flux amplitude gained by having the head very close to the disk surface, a very small head gap can generate a reliable readback voltage.

However, it takes time for the current to reverse, and the flux change is not instantaneous. Furthermore, heads must fly a finite distance from the disk. The greater the distance between the head and the oxide, the wider the head gap must be. The resulting readback voltage is more or less sinusoidal with peaks less easily defined in time or amplitude.

With modern high frequency recording techniques, adjacent clock/data pulses are close enough to interact with each other. This is shown in figure 3-54. Peak shift is the result of the interaction of the pulses. Because two pulses tend to have a portion of their individual signals superimpose themselves on each other, the actual readback voltage is the algebraic summation of the pulses.

When all "1's" or all "0's" are being recorded, the data frequency is constant: pulses are placed apart by one cell (103 nsec). As a result, the pulse spacing causes the overlap errors to be equal and opposite. The negative-going and positive-going errors cancel each other. This is the "zero peak shift" condition of the "...111..." pattern in figure 3-54.

Peak shift occurs when there is a change in frequency. A "011" pattern represents a frequency increase since there is a delay of about 1.5 cell between the "01" and only 1.0 cell between the "11". As a result, the squeezing of the cells causes the mathematical average (the actual readback voltage) to shift the apparent peak to the left. This is early peak shift.

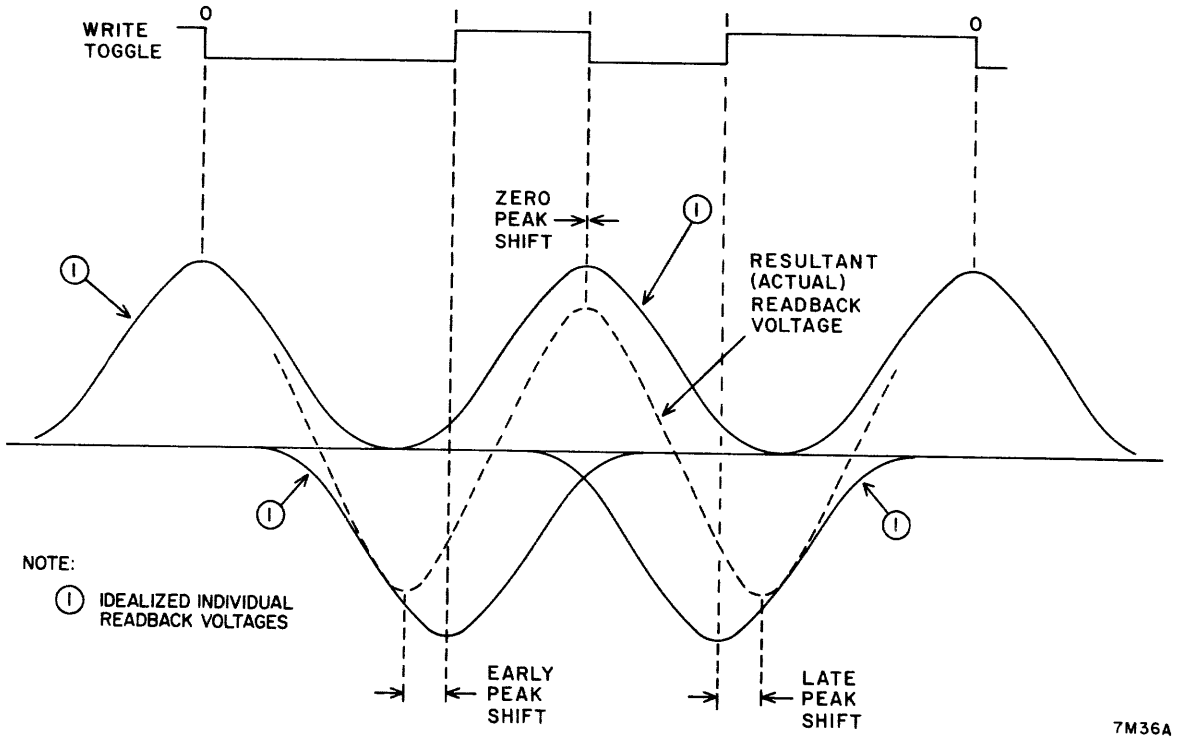


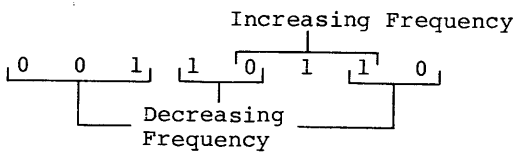
Figure 3-54. Peak Shift Timing

On the other hand, a "10" pattern represents a frequency decrease since a pulse is not written at all in the second cell. In addition, a "001" pattern is also a frequency decrease since there is a 1.0 cell interval between the first two bits and 1.5 cell between the last two bits.

The examples listed above examined only two or three bits without regard to the preceding or subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
011	Increasing
1000	Increasing
10	Decreasing
001	Decreasing

Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these eight bits:



Any of these peak shift conditions can cause errors during subsequent read operations. The drive compensates for these known errors by intentionally writing a pulse earlier or later than nominal. This function is accomplished by the write compensation circuit.

Principles of MFM Recording

In order to define the binary dibits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 nsec in width. The data transfer rate is, therefore, nominally 9.677 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (figure 3-55). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

- There is a flux transition for each "1" bit at the time of the "1".
- There is a flux transition between each pair of "0" bits.
- There is no flux transition between the bits of a "10" or "01" combination.

The advantages and disadvantages of MFM recording are as follows:

- Fewer flux reversals are needed to represent a given binary number because there are no flux reversals at the cell boundaries, achieving higher recording densities of data without increasing the number of flux reversals per inch.
- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.
- Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

READ CIRCUITS

General

Read operations are initiated by a Control tag (3) with Bus bit 1 true. This enables the analog data detection circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the read analog to digital converter which changes it into digital MFM data.

The read PLO and data separator change the MFM data to NRZ and also generate a 9.67 MHz Read Clock signal. Both data and clock are then sent to the controller.

The read circuits also detect the Address Mark area and send an Address Mark Found signal to the controller.

Figure 3-56 shows the main elements in the read circuits and table 3-7 briefly describes each of these elements. The following paragraphs further describe the read circuits.

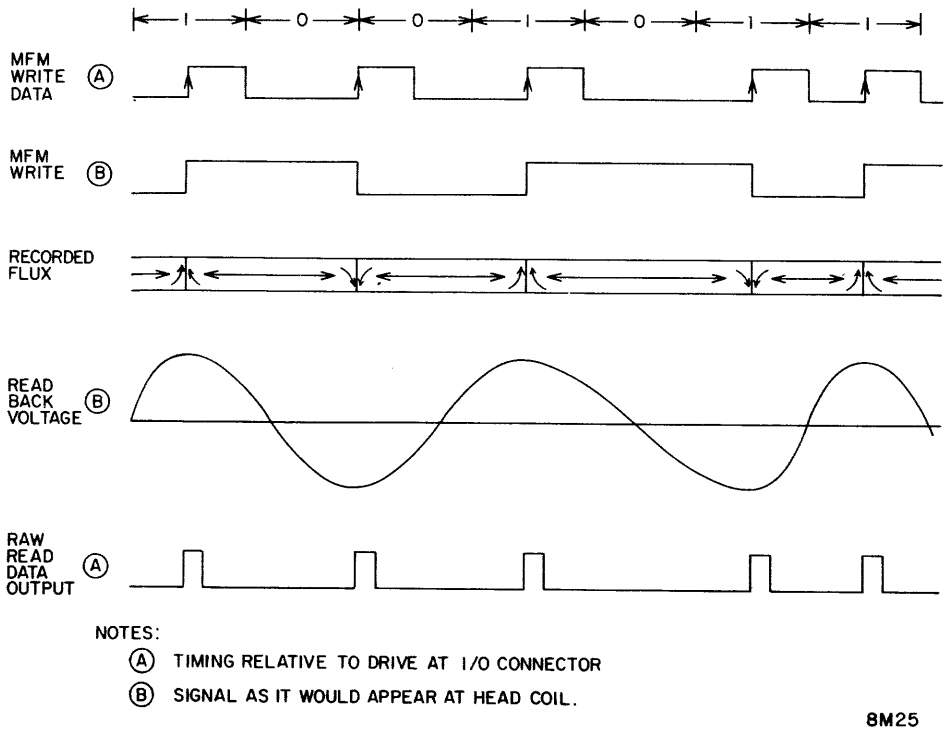


Figure 3-55. MFM Recording - Waveforms and Timing

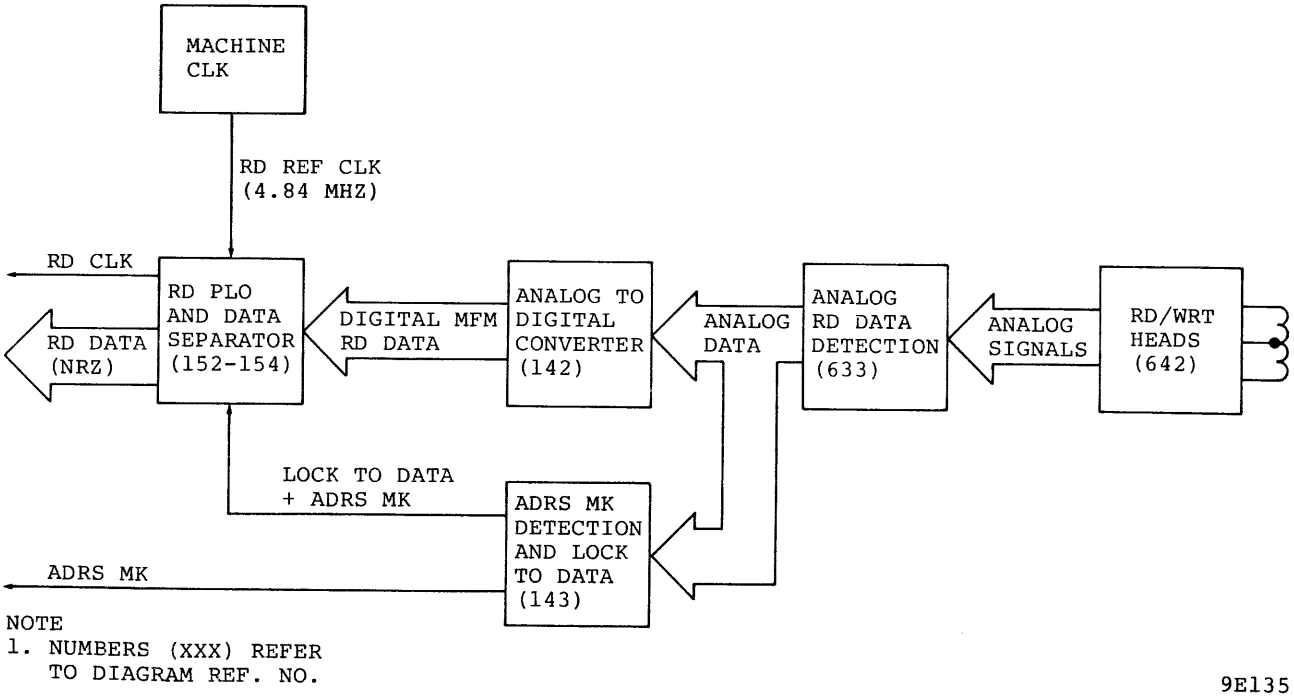


Figure 3-56. Read Circuits Block Diagram

TABLE 3-7. READ CIRCUIT FUNCTIONS

Circuit	Function
Analog Read Data Detection Circuits	Processes the analog signals sensed by the read/write heads so that they can be used by the digital to analog converter.
Digital to Analog Converter	Changes the analog MFM data into digital MFM data. This data is sent to the read PLO and data separator.
Read PLO and Data Separator	This circuit converts the MFM data to NRZ and also generates a 9.67 MHz Read Clock signal. It transmits both of these to the controller.
Address Mark Detection	Detects the Address Mark and transmits an Address Mark Found signal to the controller.

Analog Read Data Detection Circuits

The analog read data detection circuits (refer to figure 3-57) processes the analog MFM data detected from the disk so it can be used by the analog to digital converter circuits.

The Read Pre-amplifier provides preliminary amplification of the analog voltage induced in the read coil. This voltage is induced in the coil by the magnetic flux stored in the disk oxide during write operations (refer to discussion on Basic Read/Write Principles). The frequency of the analog voltage is proportional to the frequency of the magnetic field flux transitions sensed by the read coil.

The low pass filter on the output of the Read Pre-amplifier attenuates the high frequency noise on the read data signals and provides a linear phase response over the range of read data frequencies. The output of the filter is applied to the AGC amplifier. This circuit generates an output signal amplitude that remains within certain limits regardless of the amplitude of the input signal. The AGC Gain Control circuit provides the control voltage for the AGC amplifier and also provides inputs to the Address Mark detection circuits.

The Buffer amplifier processes the AGC amplifier output to provide the proper input for the analog to digital converter circuit.

Read Analog To Digital Converter

The read analog to digital converter circuits (refer to figure 3-58) receive analog MFM read data from the analog read data detection circuit and convert it to digital MFM data.

The analog to digital converter circuit consists of high and low resolution channels and the Data Latch FF. The high and low resolution channels detect the analog data by means of zero cross detectors consisting of Schmidt triggers. The zero cross detectors convert the analog data to digital pulses which are then applied to the Data Latch FF. The FF uses the outputs of both channels to produce a digital MFM data output. The low resolution channel provides the D input to the FF and the high resolution channel provides the clock. This produces an output from the Data Latch FF which retains the timing of the high resolution channel.

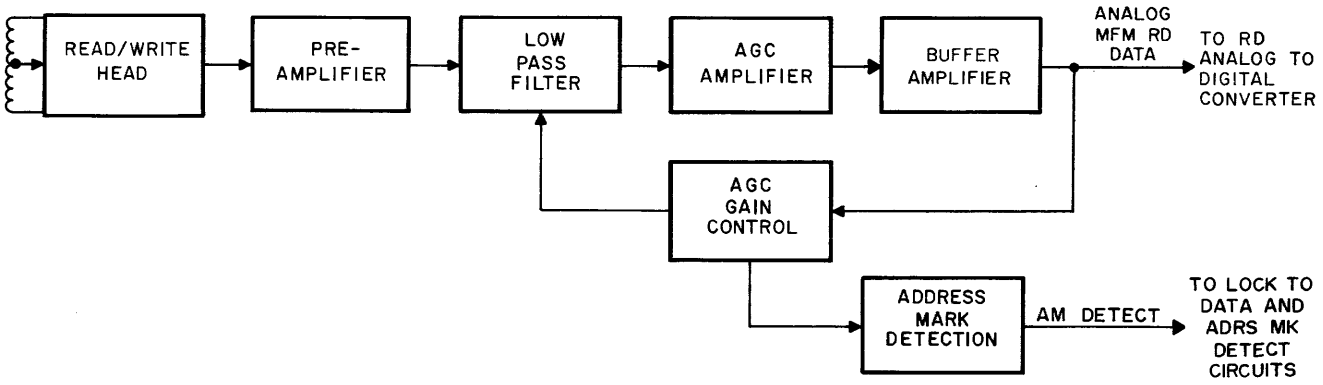


Figure 3-57. Analog Read Data Detection Circuits

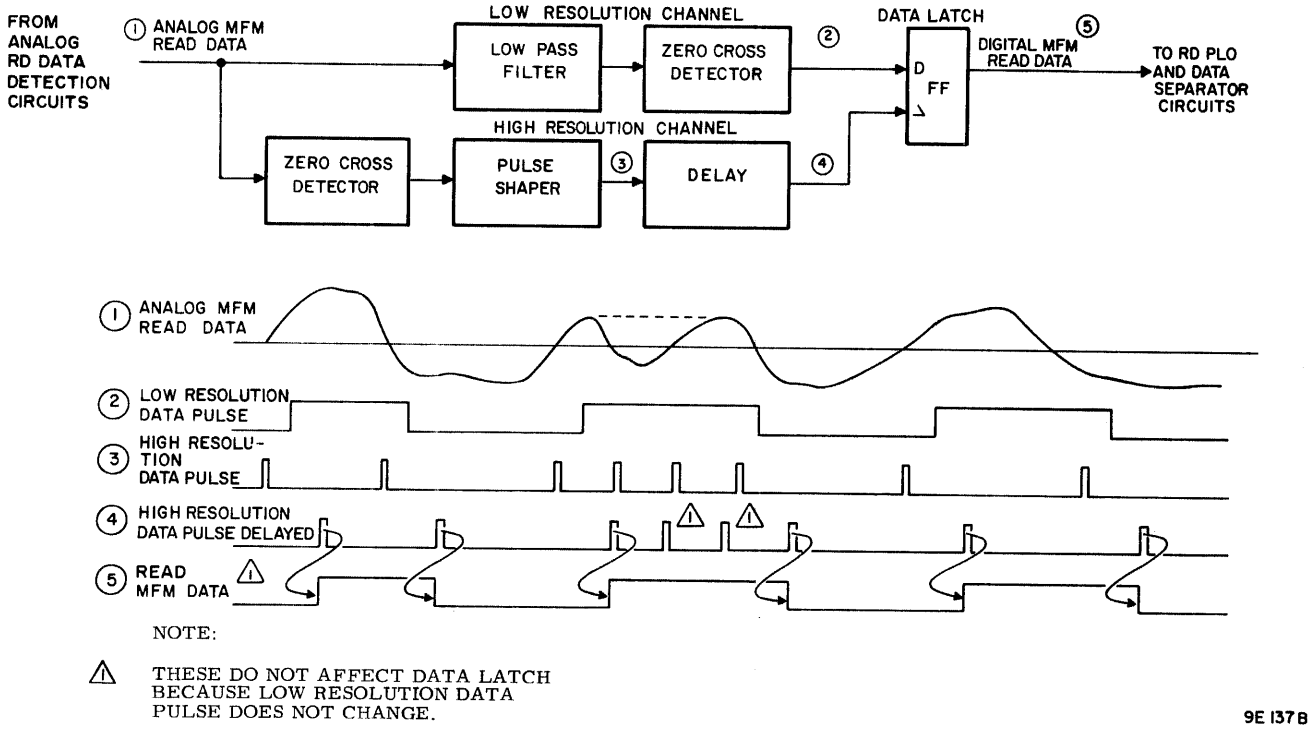


Figure 3-58. Read Analog To Digital Converter Logic and Timing

Both channels are necessary because of certain high frequency components present in the analog read data signals. These components can cause extraneous zero crossings which are detected by the zero cross detectors. However, the low pass filter in the low resolution channel attenuates the high frequency components thus eliminating any possible extraneous outputs from the channels zero crossing detector.

The high resolution channel still detects the crossings and generates clock inputs to the FF, but without the D input provided by the low resolution channel the extraneous clock pulses are ignored.

The digital MFM read data is sent to the PLO and data separator which use it to generate the NRZ data and Read clock.

Lock To Data And Address Mark Detection Circuits

These circuits generate (refer to figure 3-59) the Lock to Data signal and also detect the Address Mark area. The Lock to Data signal is used to synchronize the read PLO and data separator. The Address Mark signal is used to synchronize the read PLO and data separator and is also sent to the controller.

The Lock to Data signal is active whenever the Lock to Data one shot is in the set state. This one shot is triggered (to the set state) when either the Read Gate signal goes inactive or the Address Mark is detected.

When the Read Gate signal goes inactive it triggers the one shot and also causes it to be held in the set state. When the Read Gate signal goes active again, it removes the set conditions from the one shot and allows it to time out after 7.75 µsec. Detecting the Address Mark also triggers a 7.75 µsec pulse from the one shot. Therefore, a 7.75 µsec lock to data period occurs at the beginning of every read operation and following every Address Mark area.

The Address Mark consists of an area about 2.4 µsec in length that contains neither MFM ones or zeros. When the drive detects this area it generates a 7.75 µsec Address Mark signal.

The address mark detection circuit is enabled only during read operations (Tag 3 and Bus bit 1 active). The controller activates the circuit by raising Bus bit 5 (Address Mark Enable).

The Address Mark Enable signal causes the comparator to start generating output pulses that trigger and retrigger the Data Detect one shot. The comparator generates the output pulses only when there are input data pulses. Therefore, during the Address Mark area the comparator stops generating pulses and the one shot times out 1.7 µsec after the last data pulse was detected. The first data pulse following the Address Mark area enables the Address Mark Detect gate. This triggers the Lock to Data one shot which causes the 7.75 µsec Lock to Data and Address Mark signals to be generated.

Read PLO And Data Separator

General

This circuit has two functions: (1) to convert the MFM data from the analog to digital converter into NRZ data and (2) to generate a Read Clock signal which is locked to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signal are transmitted to the controller.

The read PLO and data separator circuits consist of four main parts (refer to figure 3-60):

- Input Control - Controls whether MFM data or 4.84 MHz clock pulses will furnish the input to the circuit.
- Data Strobe Delay - Delays the pulses to provide the proper input to the VCO. These circuits also provide error recovery capability.
- Phase Lock Loop - Synchronizes the circuit outputs to the phase and frequency of the inputs.
- Data Separator - Converts the MFM data to NRZ data and generates the Read clock. This circuit is actually a part of the phase lock loop.

The remainder of this discussion further describes the read PLO and data separator circuits.

Input Control

The input control circuit (refer to figure 3-60) selects the input that will be used by the read PLO and data separator circuits. This input will always be either MFM data from the read analog to digital converter or 4.84 MHz clock pulses from the servo frequency multiplier circuit.

The 4.84 MHz clock signal is used only when the drive is not reading MFM data, such as before Read Gate is raised. It also uses the 4.84 MHz clock whenever the Address Mark Enable signal is active because this indicates the drive is expecting the Address Mark which contains no MFM data. The drive

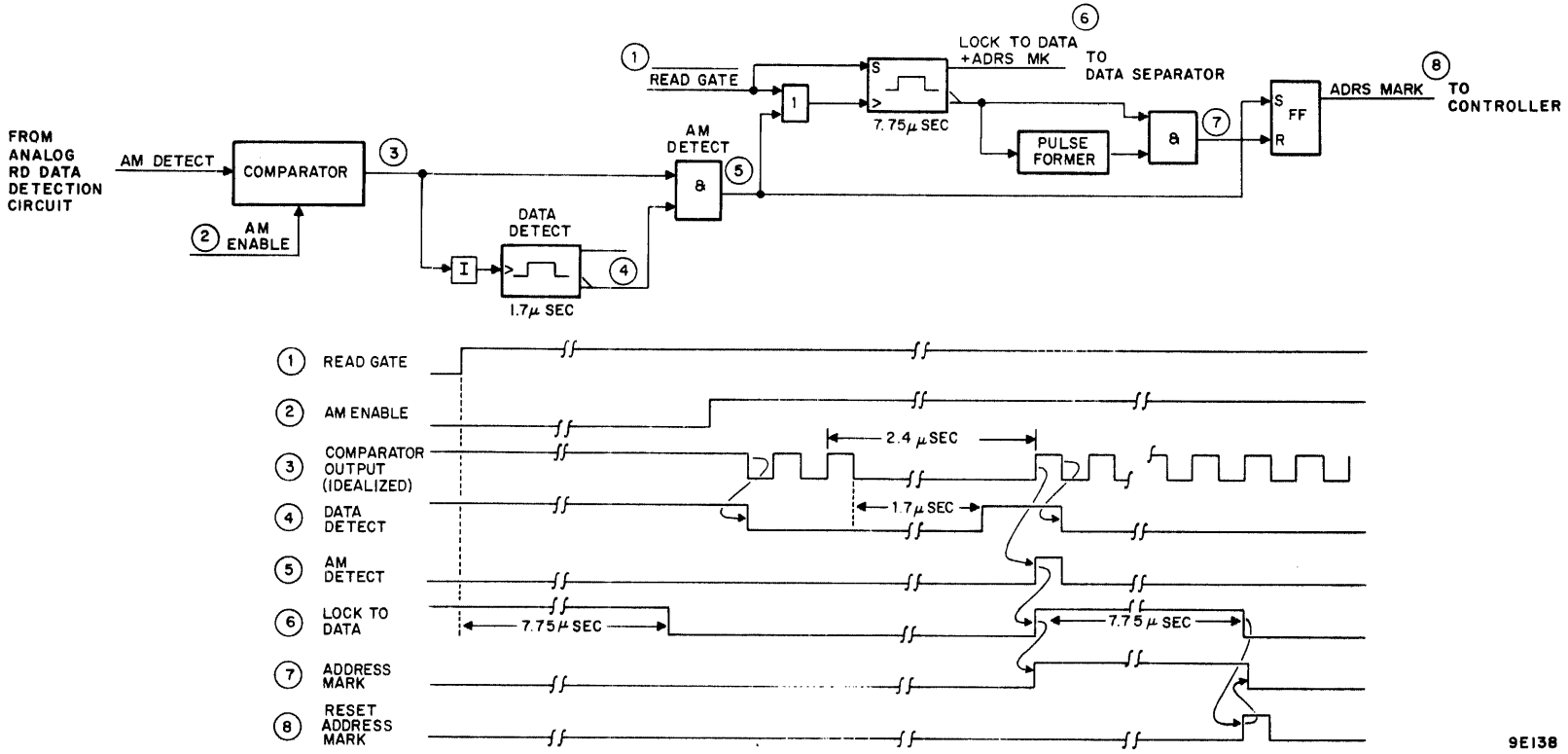


Figure 3-59. Lock to Data/Address Mark Detection Logic and Timing

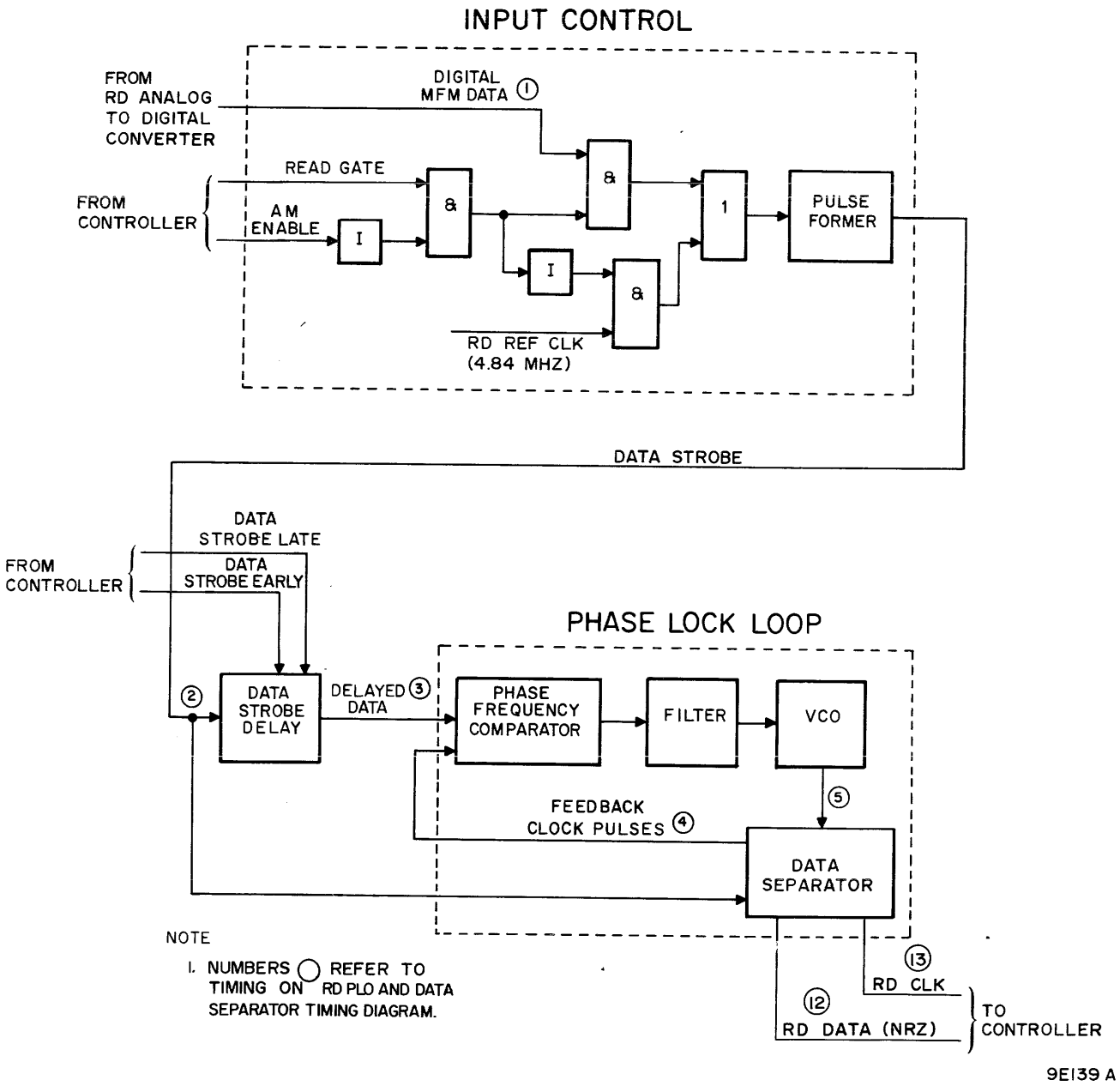


Figure 3-60. Read PLO and Data Separator Circuits

uses the clock signal as a substitute for the read data for two reasons: (1) the signal is derived from the track servo dibits and therefore, its frequency (like that of the read data) varies directly with disk pack speed and (2) after being processed by the pulse forming circuits, it has about the same nominal frequency as the read data (9.67 MHz). This results in it being easier for the phase lock loop to synchronize to the proper frequency when switching from one of the signals to the other.

Once selected the signal is applied to a pulse forming network which generates a 20 nsec pulse for each transition of the input. These pulses are then applied to the data strobe delay circuits and also furnish the data input to the data separator.

Data Strobe Delay

The purpose of the data strobe delay circuit (refer to figure 3-60) is to delay the data pulses sufficiently to provide the proper timing relationship at the input to the phase lock loop. The output of the data strobe delay circuit is delayed by a time determined by the state of the Data Strobe Early and Data Strobe Late signals. These signals facilitate the recovery of marginal data and are enabled by Data Strobe Early or Late (Bus Bit 7 or 8) and Control Tag (3).

The output of this circuit is the Delayed Data signals which are sent to the input of the phase lock loop.

Phase Lock Loop

The phase lock loop (refer to figure 3-60) synchronizes the read PLO/data separator circuit outputs (NRZ data and Read Clock) to the input (either MFM data or 4.84 MHz clock). The loop accomplishes this by comparing and following two signals: (1) the Delayed Data signals which have a constant phase and frequency relationship to the input MFM data or 4.84 MHz Clock (whichever is used) and (2) the Feedback Clock Pulse signals which have a constant phase and frequency relationship to the output NRZ data and Read Clock signals. The loop inputs are applied to the phase/frequency comparator.

The phase/frequency comparator generates output pulses which are a function of the phase and frequency between the positive going edges of the inputs. The filter circuit uses the comparator outputs to generate a control voltage for the voltage controlled oscillator (VCO).

This control voltage causes the frequency of the VCO to vary in the direction necessary to eliminate the phase and frequency differences between the two signals that were input to the comparator.

The output frequency of the VCO is actually twice that of the input so for an input of 9.67 MHz it has an output of 19.34 MHz. However, the data separator divides this by two before generating the Feedback Clock Pulse signals thereby providing a feedback to the comparator that satisfies the loop.

Data Separator

This circuit determines if the data pulses represent a one or zero and then converts the data to NRZ. It also generates the Feedback Clock Pulses to the comparator and the 9.67 MHz Read Clock that is sent to the controller. Figures 3-61 and 3-62 show simplified logic and timing for the data separator circuit.

The VCO outputs provide the proper timing relationships for the data separator by controlling the Data Window and Read Clock FFs. The Read Clock FF generates the 9.67 MHz Read Clock signal and also provides timing signals to the data separator logic. The Data Window FF generates the Data window which is used to determine whether the input data pulses represent ones or zeros. The actual decoding of the data is done by the "1's" Enable and "0's" Enable FFs.

If a data pulse represents a one it occurs during the data window and sets the "1's" Enable FF. Setting this FF generates a Feedback Clock pulse and causes the Data Buffer FF to generate a NRZ one.

If the data pulse represents a zero the "1's" Enable FF is not set and the Data Buffer FF generates a NRZ zero. In this case the "0's" Enable FF which is set by every data pulse generates the Feedback Clock Pulse signal.

Before accurate detection of data can begin, the proper phase relationship must be established between the data (representing ones and zeros) and the VCO output pulses. This is done during a 7.75 µsec lock to data period which is initiated by the Lock to Data signal. This signal is a 7.75 µsec pulse that occurs when the Read Gate signal goes true or when the Address Mark is detected. The Lock to Data signal holds the "0's" Enable FF set and disables the output of the "1's" Enable FF. Therefore, if the circuit is to synchronize properly the pulse must occur during a period when the drive is reading only zeros.

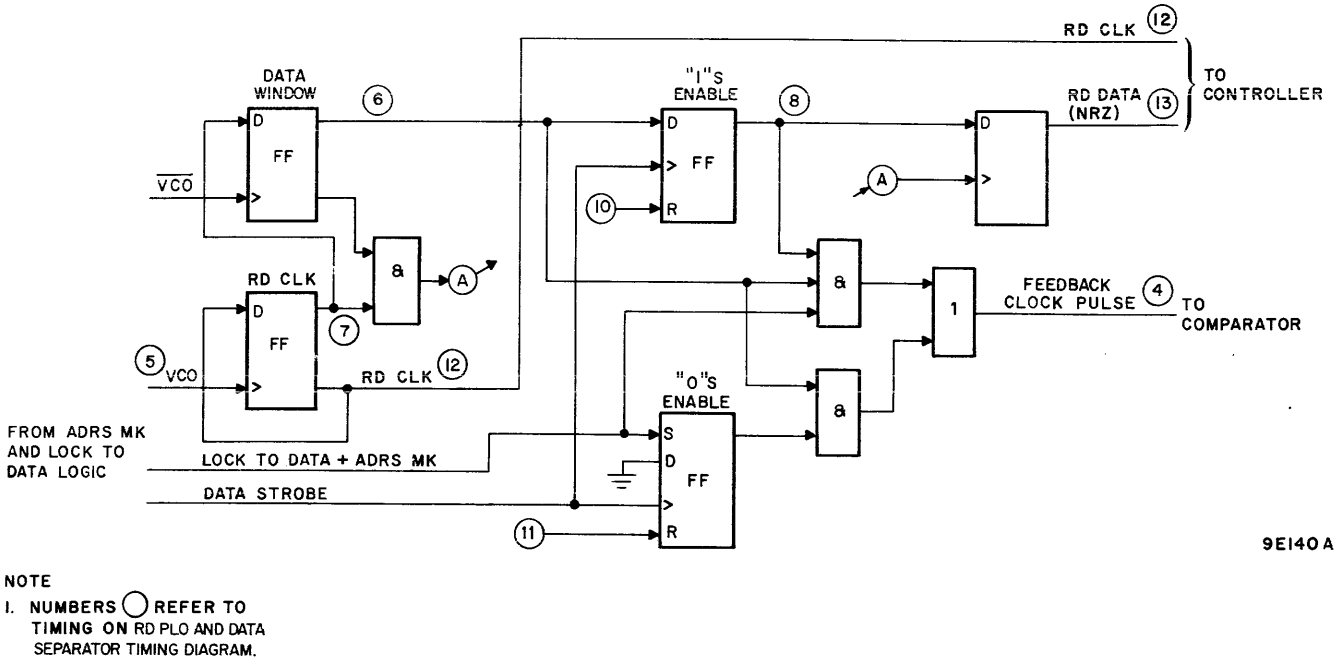


Figure 3-61. Data Separator Logic

WRITE CIRCUITS

General

The Write circuits operation is initiated by a Control tag (3) with Bus bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. The write data is received via the bi-directional Read/Write data line and is first sent to the RNZ to MFM converter/ write compensation circuits. These circuits convert the data to MFM and also compensate it for peak shift (refer to discussion on basic read/write principles for more concerning peak shift). The compensated data is then processed by the write drive circuits and written on the disk.

Figure 3-63 shows the write circuits and table 3-8 briefly explains their function.

NRZ to MFM Converter/Write Compensation Circuits

The NRZ to MFM Converter/Write Compensation circuits convert the NRZ data into MFM data and also shift the output MFM pulses to compensate for peak shift (refer to discussion on basic read/write principles). Figures 3-64 and 3-65 show simplified logic and timing for these circuits.

The 9.67 MHz and 19.34 MHz signals from the servo frequency multiplier circuit provide basic timing signals for the write compensation circuits. The NRZ data from the controller provides the data input. These inputs are applied to the pattern decode and NRZ to MFM converter circuits.

The NRZ to MFM converter converts the NRZ data, into MFM data and applies it to a delay line. The delay line has three outputs which are combined with the outputs of the pattern decode logic (at the Early, Late and Nominal gates) to produce compensated write data.

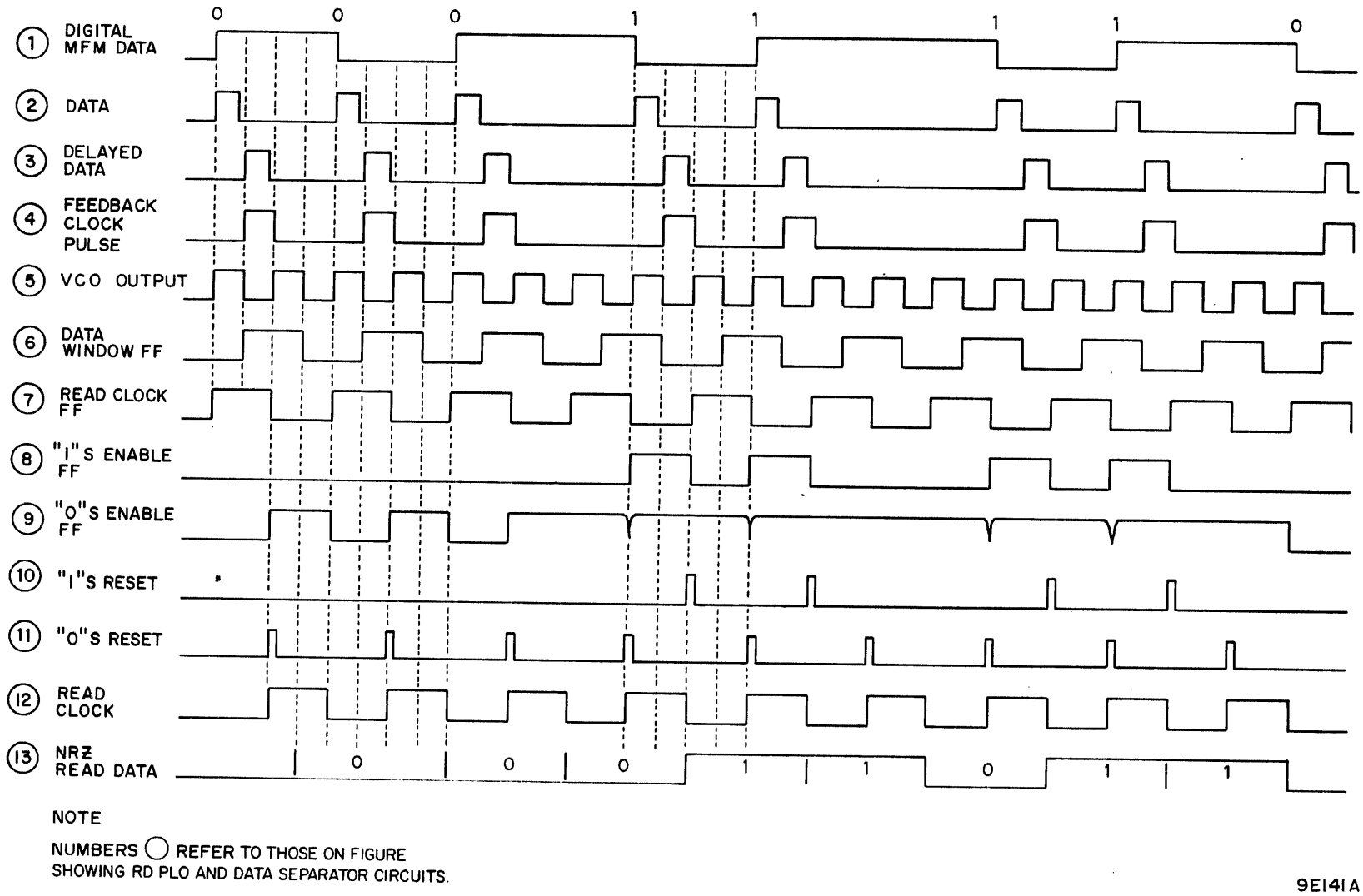


Figure 3-62. RD PLO and Data Separator Timing

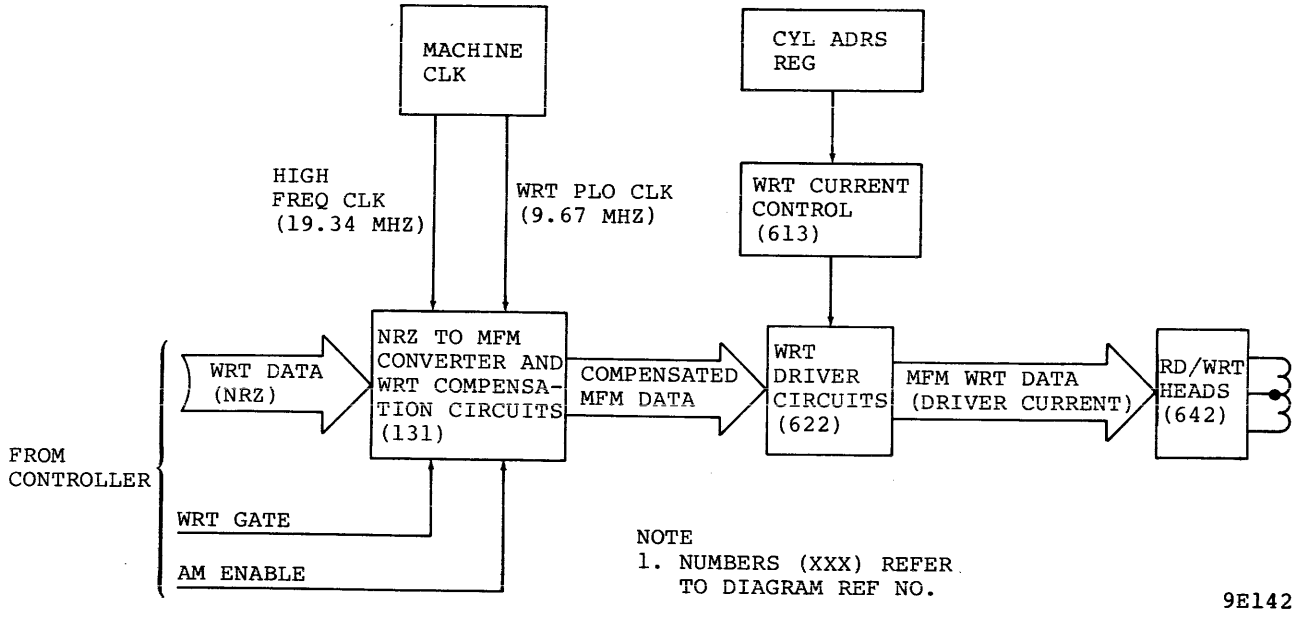


Figure 3-63. Write Circuits Block Diagram

TABLE 3-8. WRITE CIRCUIT FUNCTIONS

Circuit	Function
NRZ to MFM Converter and Write Compensation Circuits	Converts the NRZ data from the controller to MFM data and also compensates the data for problems caused by variations in the write data frequency.
Write Driver Circuits	Uses the MFM data to produce the current necessary to record data on the disk.
Write Current Control	Reduces the write current amplitude as the heads move from the outer tracks to inner tracks. This assures that the correct amount of current will be used as the circumference of the cylinders decrease.

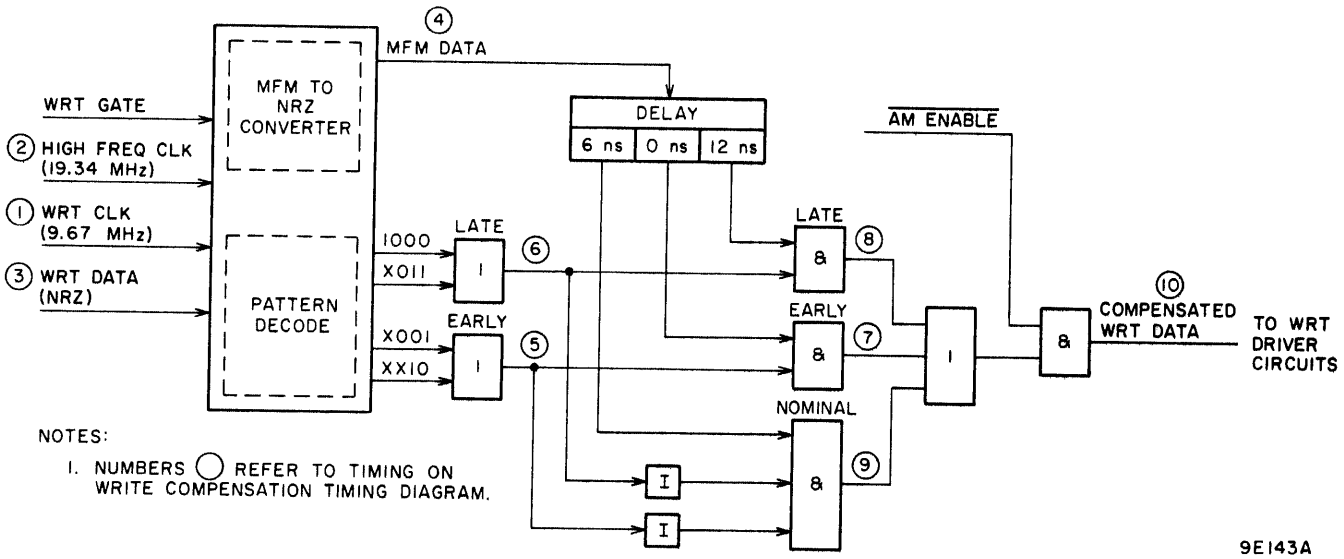


Figure 3-64. Write Compensation/NRZ to MFM Converter Circuits

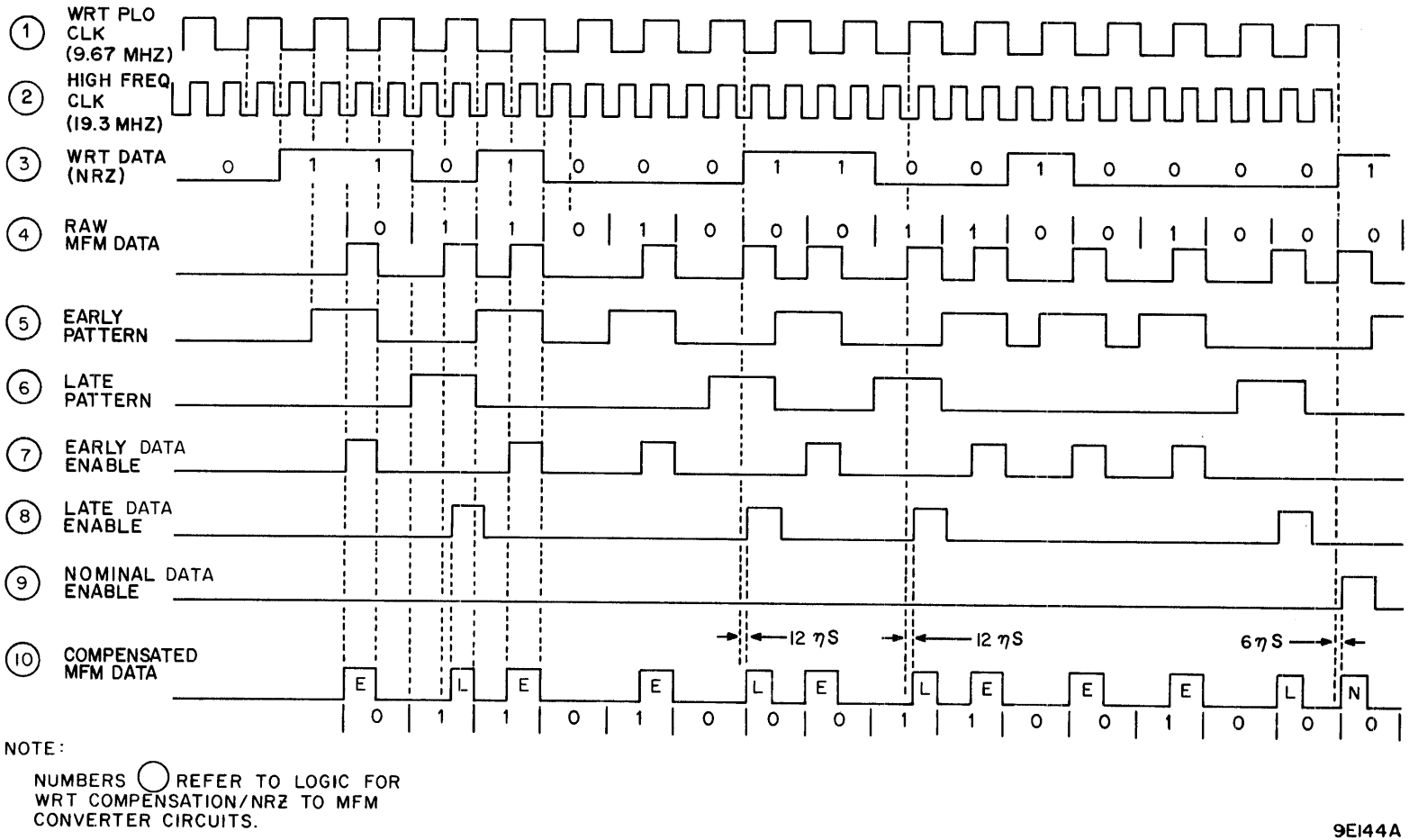


Figure 3-65. Write Compensation Timing

The pattern decode logic analyses the NRZ data and determines if its frequency is constant (00000 or 11111), increasing (011 or 1000), or decreasing (10 or 001). The outputs from the pattern decode logic enable either the Early, Late or Nominal gate (depending on the input frequence) to provide compensated Write data as follows:

- If frequency is constant, there will be no peak shift. In this case the data is defined as nominal and is delayed 6 nsec.
- If frequency is decreasing, the apparent readback peak would occur later than nominal. To compensate for this, the data is not delayed and is therefore 6 nsec earlier than the nominal data.
- If frequency is increasing, the apparent readback peak would occur earlier than nominal. Therefore, this data is delayed 12 nsec which is 6 nsec later than nominal.

After being write compensated the data is transmitted to the write driver circuits.

Write Driver Circuit

The compensated write data is sent to the read/write chassis and applied to a differential receiver in the write driver circuits (refer to figure 3-66). The output of the receiver then serves as a clock for the Write Toggle FF. This flip flop toggles only when the Write Enable signal is active. The output of this flip flop provide the input to the Write Driver which in turn generates the current for the read/write heads. The magnitude of the current applied to the heads is controlled by the write current control circuits.

Write Current Control

The magnitude of the write current sent to the heads is controlled as a function of cylinder address. This is referred to as write current zoning as the zones are divided into the following segments of tracks: 0-127, 128-255, 256-511, and 512 through 822. Write current is reduced at each zone boundary from outer to inner tracks.

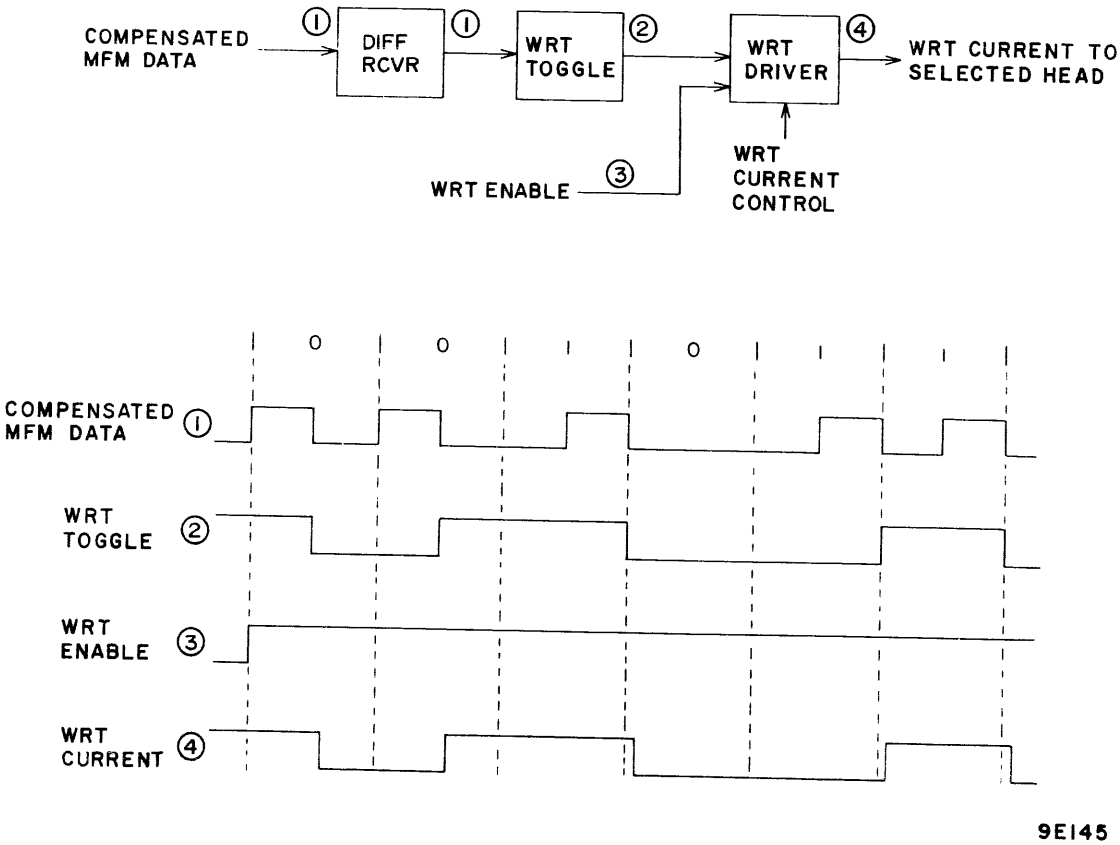


Figure 3-66. Write Driver Circuits and Timing

Writing Address Marks

The Address Mark is an area that contains neither MFM "1's" or "0's". The drive starts writing an Address Mark when it receives Tag 3 and Bus bits 0 and 5 from the controller. This activates the Address Mark Enable signal which prevents compensated write data from going to the write driver circuits. The Write Driver continues to generate current for the write coil but without data no current reversals occur. The effect is to erase all information from the disk. The drive stops writing the Address Mark when the controller drops Tag 3 Bus bits 0 or 5.

Write Data Protection

General

Write data protection consists of disabling the write driver circuit whenever there is danger of writing faulty data on the disk pack. It is initiated if the drive detects the Write Protect signal active, Fault latch set, or a low voltage condition. All of these are described in the following.

Write Protect

The Write Protect signal goes active if any of the following occurs.

- Controller commands a write while the heads are in an offset position (refer to discussion on Direct Seek Fine Position Control-Track Following).
- WRITE PROTECT switch on drive operator panel has been depressed to light the indicator. In this case, depressing the switch to extinguish the indicator causes the Write Protect signal to go inactive.
- Head alignment is being performed.
- Low dc voltage condition is detected or the disk pack speed slows down below 2700 r/min. Both of these conditions will also cause an emergency retract of the heads (refer to discussion on (Emergency Retract).

Fault

The Fault latch sets as a result of a number of drive malfunctions. The conditions causing the Fault latch to set are described in the discussion on Fault and Error Conditions.

Loss of Voltage

If power is lost or drops below a certain level, an emergency retract is performed. However, in this case it is possible that other signals used to disable the write driver (Write Protect and Fault) will not function properly and the drive will continue to write while the heads are being retracted. This could alter or destroy data already on the pack. The loss of voltage protection circuit consists of a capacitive discharge network that ensures the write circuits are disabled until the heads are unloaded.

FAULT AND ERROR CONDITIONS

GENERAL

The following describes those conditions which are interpreted by the drive as errors. All of these conditions either light an indicator at the drive and/or send a signal to the controller indicating an error has occurred.

These errors are divided into two categories: (1) those indicated by Fault Latch and register (2) those not indicated by Fault Latch and register. Both are explained in the following (refer to figure 3-67).

ERRORS INDICATED BY FAULT LATCH AND REGISTER

General

Certain errors set the drives Fault latch and also set the fault register latches associated with the error condition.

Setting the Fault Latch does four things (1) enables the fault line to the controller (2) lights the FAULT indicator on the drives operator control panel (3) clears the drives Unit Ready signal (4) inhibits the drives write and load circuitry. These events prevent further drive operations from being performed until the error is corrected and the Fault latch is cleared.

Providing the error condition or conditions no longer exist, the Fault latch is cleared by any of the following

- FAULT switch on operator panel.
- Controller Fault Clear signal from the controller.

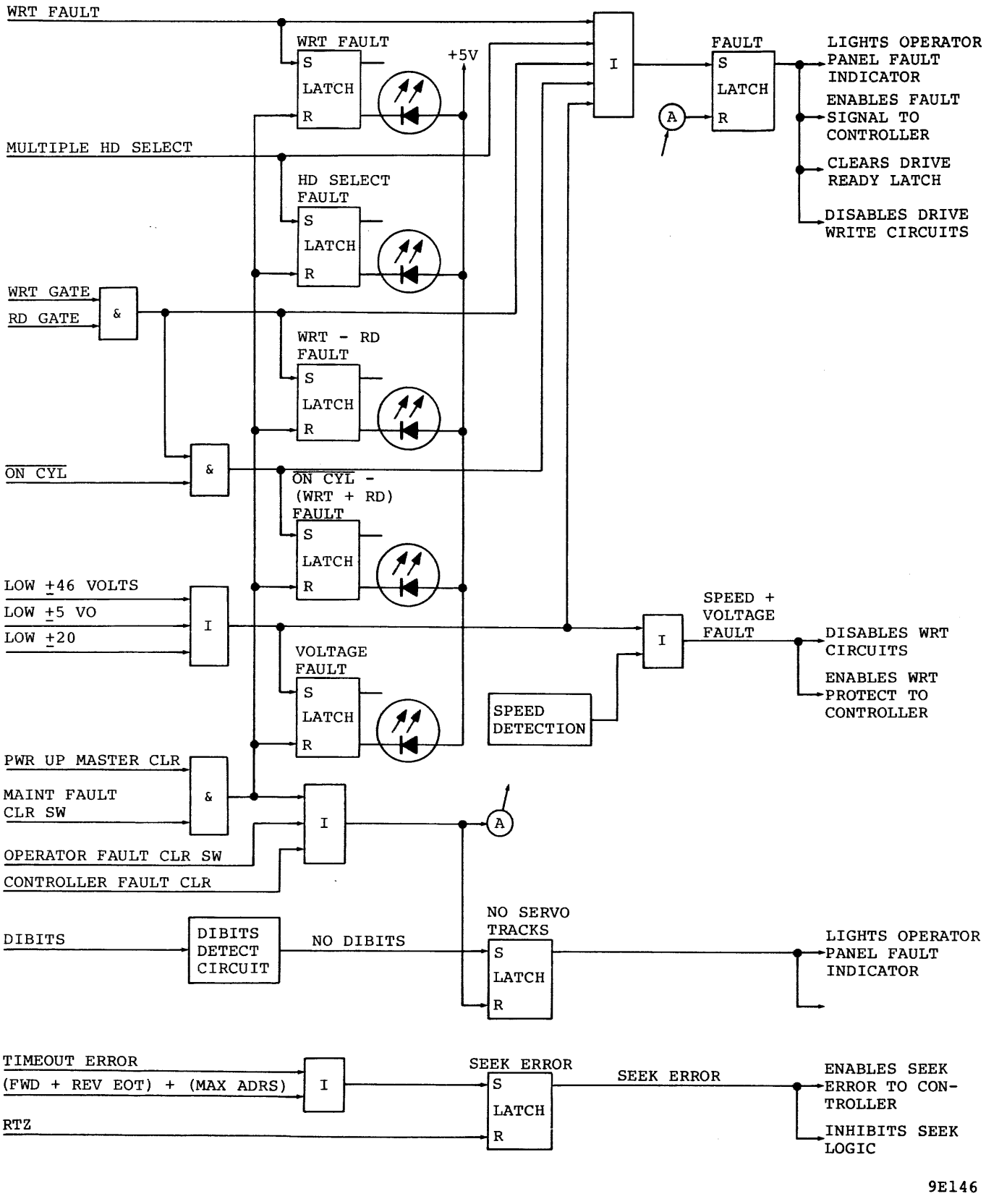


Figure 3-67. Fault and Error Detection Logic

- Maintenance Fault Clear switch on Fault card.
- Powering down the unit.

Whenever an error occurs that sets the Fault latch, it also sets a latch in the fault register. These latches provide a means of storing the error indication unit so it can be referred to later for maintenance purposes. The fault register latches are cleared only by powering down the drive or by the Maintenance Fault Clear switch on the fault card.

The following describes each of the conditions causing the Fault latch and fault register latches to be set.

Write Fault

A write fault is indicated if any of the following conditions exist.

- Low output from write driver indicating it may not be operating properly.
- Low current input to write driver.
- Low +22 volts to write driver.
- No write data transitions when Write Gate is active.

More Than One Head Selected

This fault is generated whenever more than one head is selected. The outputs of the head select circuits are monitored by summing and voltage comparator circuits. If more than one head is selected, the circuit generates a Multiple Select Fault.

Read and Write

This fault is generated whenever the drive receives a Read gate and Write gate simultaneously from the controller.

(Read or Write) and Off Cylinder

This fault is generated if the drive is in an Off Cylinder condition and it receives a Read or Write gate from the controller.

Voltage Fault

This fault is generated whenever the ±46, ±5 or ±20 voltages are below satisfactory operating levels.

ERRORS NOT INDICATED BY FAULT LATCH OR REGISTER

General

The following errors are detected by the drive but are not stored in the fault register and do not set the Fault latch. However, they do sense the drive to give other error indications and this is explained in the following paragraphs.

Low Speed or Voltage

The Speed or Voltage Fault signal goes true when the drive detects either a low voltage condition or that drive spindle speed is below 2700 r/min. When either of these are detected, the drive write circuits are disabled and the Write Protect signal is sent to the controller. These also result in an emergency retract of the heads (refer to discussion on Emergency Retract).

No Servo Tracks Fault

If dibits are not detected within 350 ms after the load seek sequence begins, the No Servo Tracks latch is set. This lights the FAULT indicator on the drive operator control panel and also enables the Return to Zero (RTZS) logic. Enabling the RTZS logic causes the heads to unload. Another load cannot be started until the No Servo Tracks latch is cleared. The No Servo Tracks latch is cleared in the same manner as the Fault latch.

Seek Error

The Seek Error latch is set by any of the following error conditions:

- On Cylinder was not obtained within 500 ms from the start of the seek.
- Forward or reverse end of travel (EOT) sensed.
- Drive is commanded to seek to a cylinder address greater than 822 (410).

Setting the Seek Error latch enables the Seek Error line to the controller and also inhibits the drive from performing another seek until the Seek Error latch is cleared. The latch is cleared by a Return to Zero Seek command.

SECTION 4

DISCRETE COMPONENT CIRCUITS

GENERAL

This section contains a circuit description for each type of discrete component circuit used in various drive models covered in this manual. These circuits use discrete components mounted on a card, and form specialized logical or analog functions for which no integrated circuit is available. Figure 6-1 is a typical example of the manner in which discrete component circuits are presented in this section. A schematic is provided along with the logic symbol for that circuit as it would appear in the logic diagrams manual. Only the circuit function (▷ , amplifier in this case) and the circuit-type designator are shown within the logic symbols in this section. The circuit type, HAB, for instance denotes a high-level amplifier.

Numbers on the input and output lines indicate which transistors are being driven or which are acting as drivers. The brackets inside the symbol at both the input and output lines denote that those lines are differentials. A slash on any line shows that the signal level is a non-standard logic level.

Presentation of the circuit descriptions in this section is by the three-letter circuit type designator in alphabetical order.

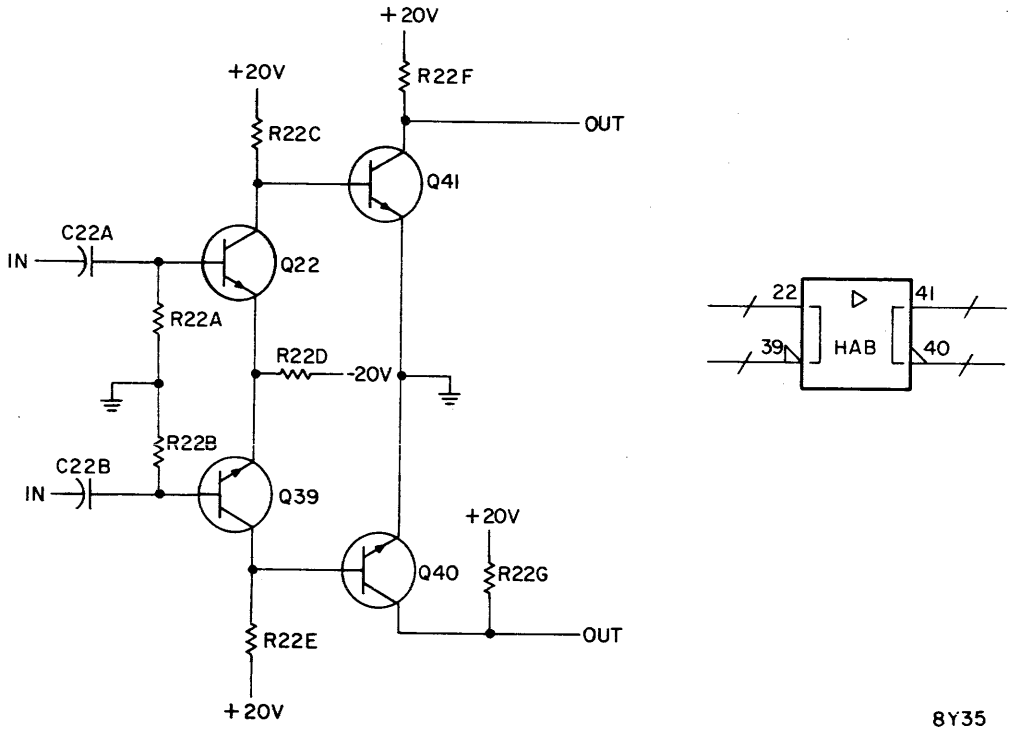


Figure 6-1. Typical Discrete Component Circuit Schematic

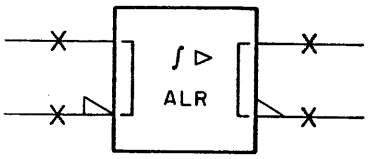
Amplifier and Filter - ALR

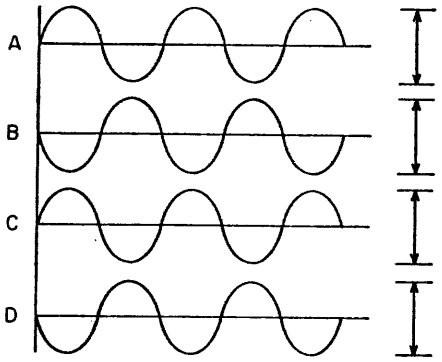
The ALR circuit is a differential amplifier and a 2 pole linear phase filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 2.

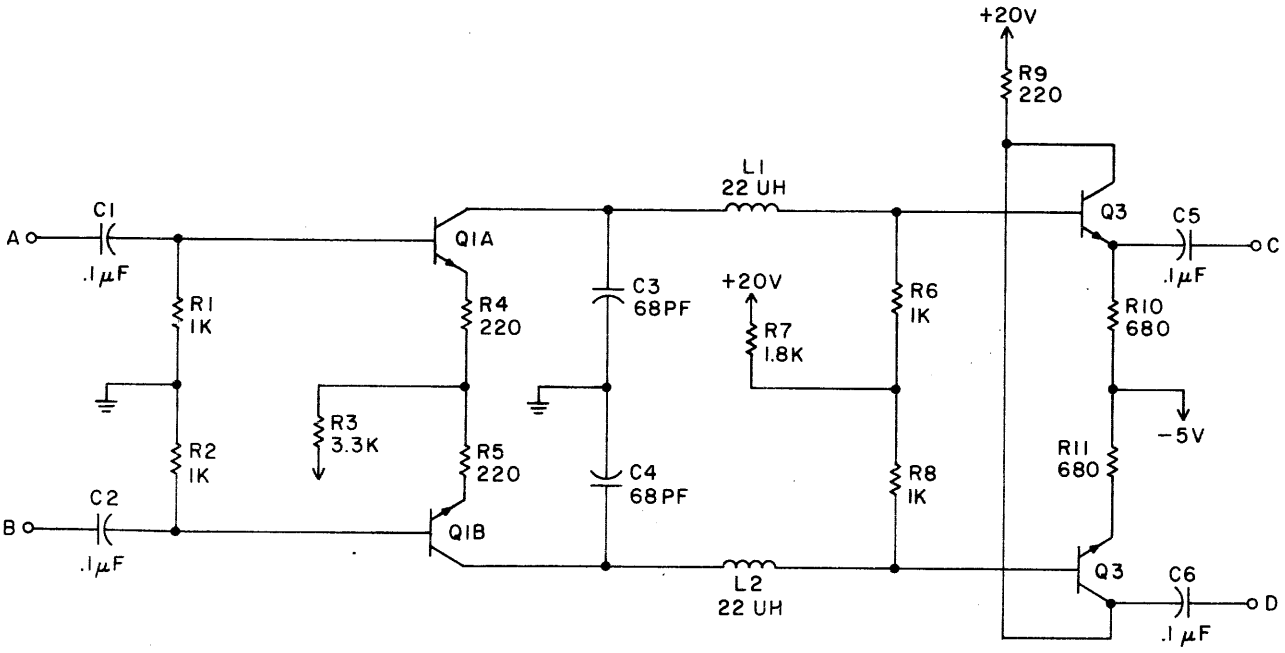
Q1A and B form the differential amp with R6 and R8 being the load resistors and also impedance matching resistors for the filter. The inductors L1 and L2 and capacitors C3 and C4 make up the rest of the filter. The upper break design frequence (-3 db point) of the filter is 3.13 MHz.

The input coupling capacitors C1 and 2 in conjunction with bias resistors R1 and 2 give the circuit a low frequency cutoff (-3 db point) of less than 2 kHz.

The output is a differential emitter follower buffer consisting of Q3 and 4 and R10 and 11, that is used to reduce the output impedance.







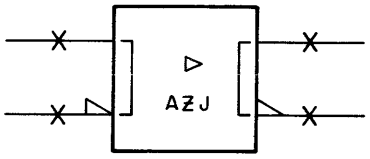
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

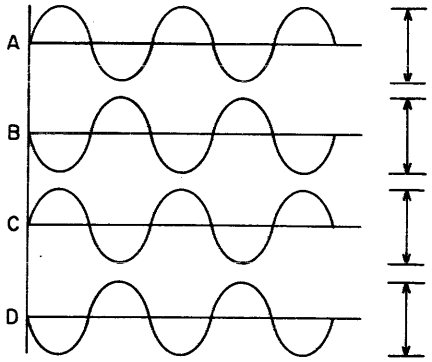
ALR
Rev A
Sheet 1 of 1

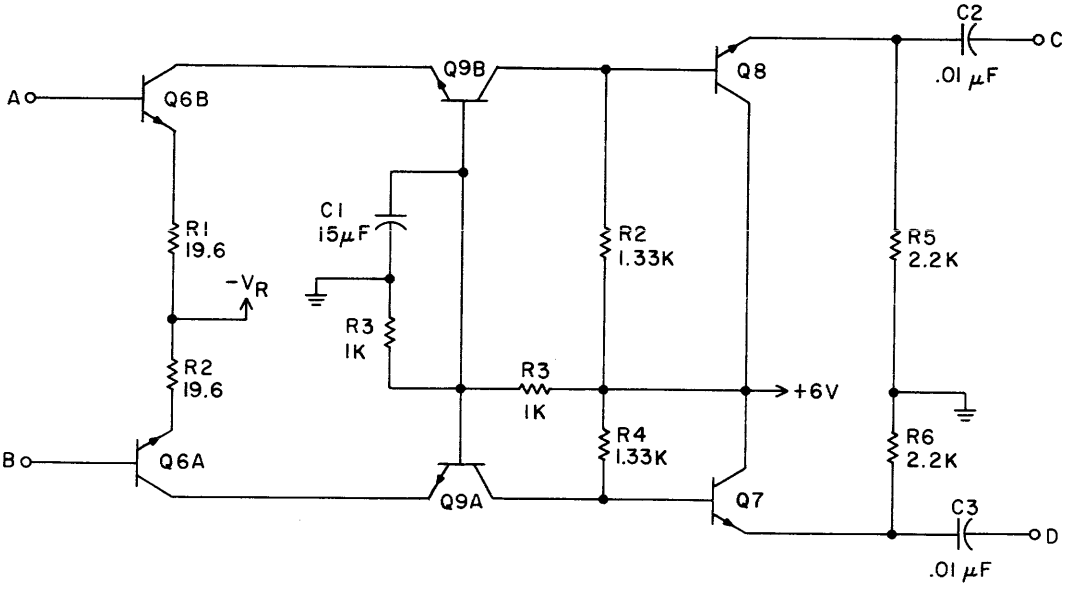
Differential Amplifier - AZJ

The preamplifier is a cascade type with a matched pain of transistors (Q6A and Q6B) used as a common emitter front end followed by another matched pain of transistors (Q9A and Q9B) used as a common base second stage, this effectively reduces the emitter collector capacitance of the common emitter front end.

The final stage of the front end is a emitter follower (Q7 and Q8) used as a buffer between the preamp and filter section. Resistors R1 and R2 in the emitter circuit give the front end a input impedance of just under the 500 ohms. The constant current source for the preamp supplies approximately 2.5 ma.







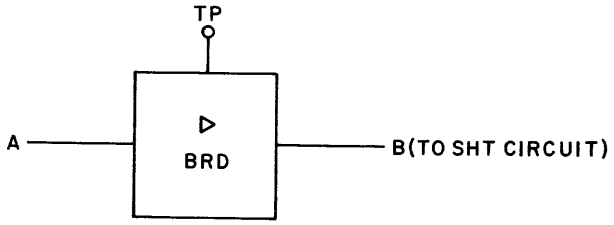
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

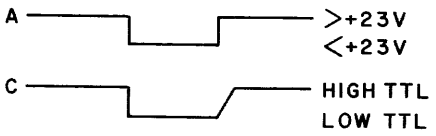
AZJ
Rev A
Sheet 1 of 1

LEVEL TRANSLATOR (COMPARATOR SECTION) - BRD

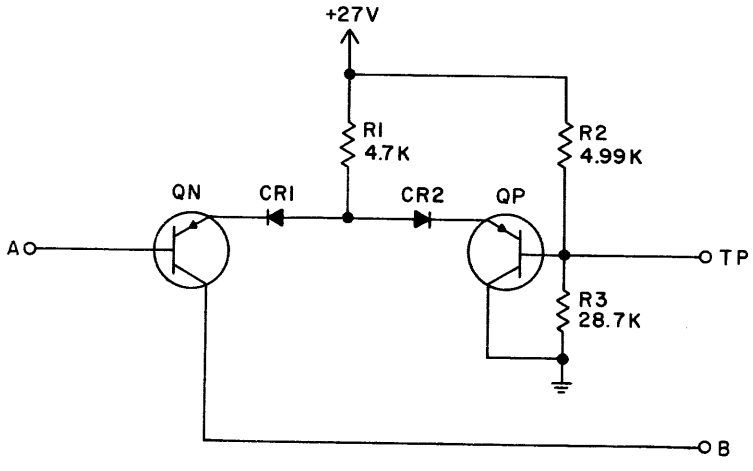
The BRD circuit is a differential voltage comparator which operates in conjunction with the SHT circuit to translate input signal levels of below +23 V to a low TTL output and input signal levels of above +23 V to a high TTL output.

The BRD circuit functions in conjunction with the SHT circuit to indicate whether or not the write current is below a minimum value. (See SHT circuit description.) A voltage reference of +23 V is applied to the base of transistor QP. With normal write current, the base of QN is below +23 V. Under these conditions transistor QN is on and transistor QP is off, and the resistor in the collector circuit of QN provides a forward bias voltage to the SHT circuit. If the write current is below the acceptable minimum, the voltage at the base of QN goes above +23 V. Then QN turns off and QP turns on, and the resistor in the collector circuit of QN does not develop sufficient forward bias for the SHT circuit.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BRD
Rev B
Sheet 1 of 1

Amplifier and Filter - BZJ

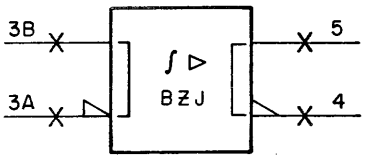
The BZJ circuit is a differential amplifier and a 4 pole low pass Butterworth filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 7.5.

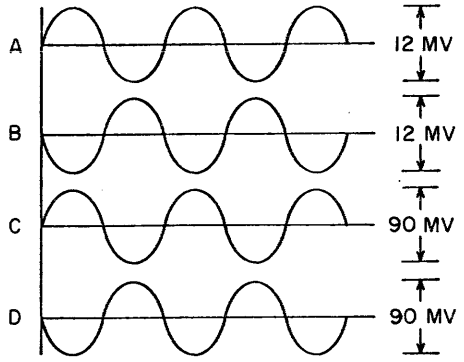
Q3A and B form the differential amplifier with R5 and R6 being the load resistors and also impedance matching resistors for the filter. The inductors L1, L2, L3, and L4 and capacitors C1, C2, C3 and C4 make up the rest of the filter. The upper break frequency (-3db point) of the filter is approximately 6.8 MHz.

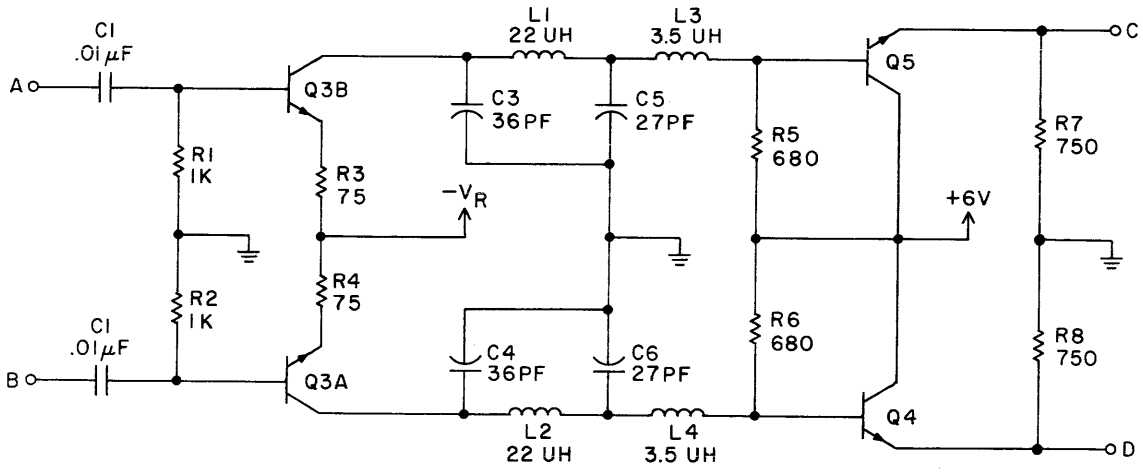
The input capacitors C1 and C2 in conjunction with resistors R1 and R2 give the circuit a low frequency cutoff (-3 db point) of less than 20 kHz.

The output is a differential buffer consisting of Q4, Q5, R7, and R8 that is used to reduce the output impedance and give more drive.

The constant current source for the differential amp supplies approximately 4.75 ma.



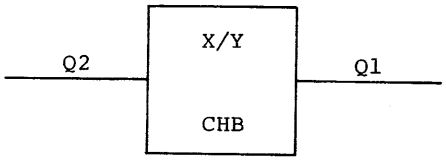


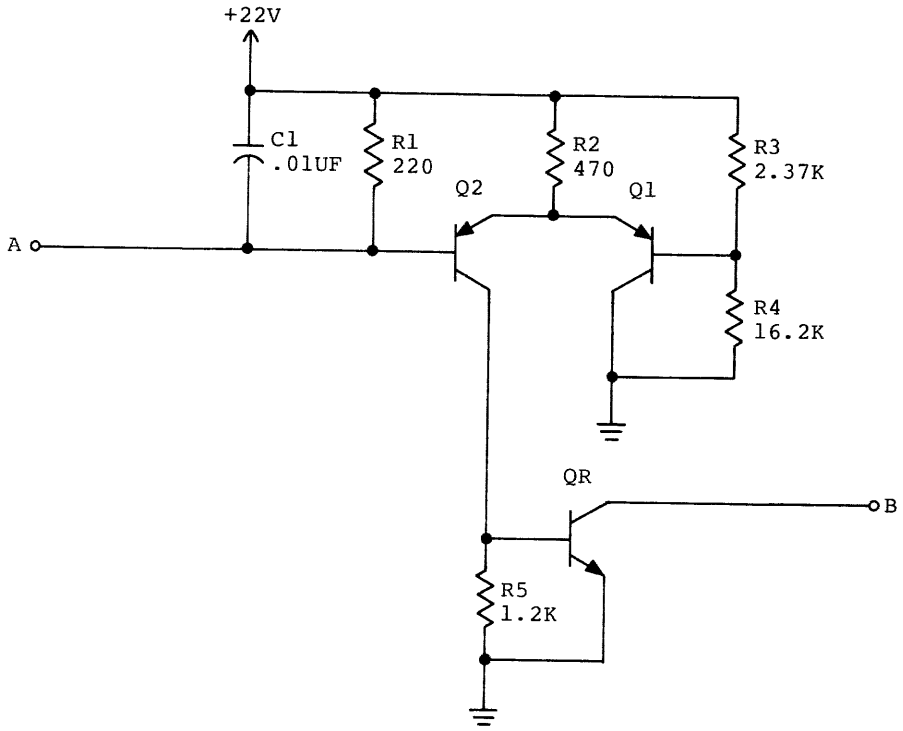


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BZJ
Rev A
Sheet 1 of 1

Circuit functional description will be included in a later revision.

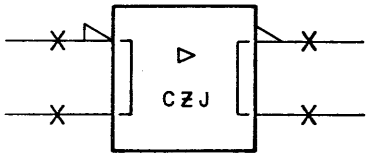


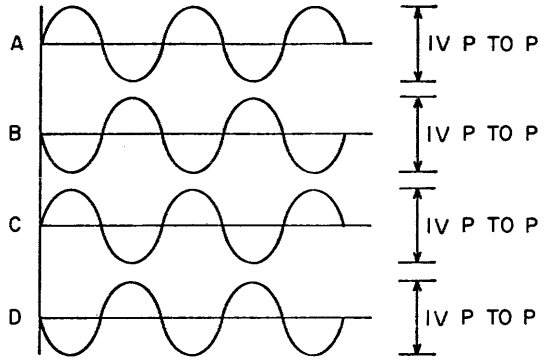


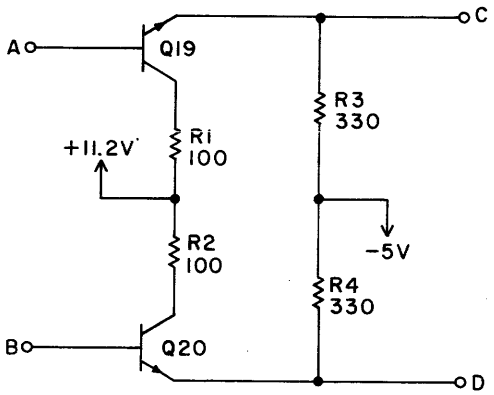
CHB
Rev A
Sheet 1 of 1

BUFFER AMPLIFIER - CZJ

The CZJ circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal. Q19 and Q20 are emitter followers that present comparatively high input impedance and low output impedance.







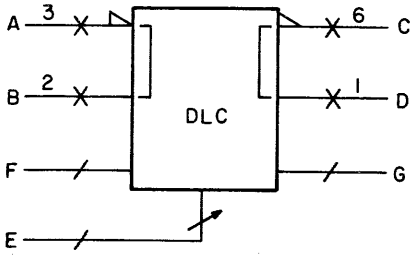
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

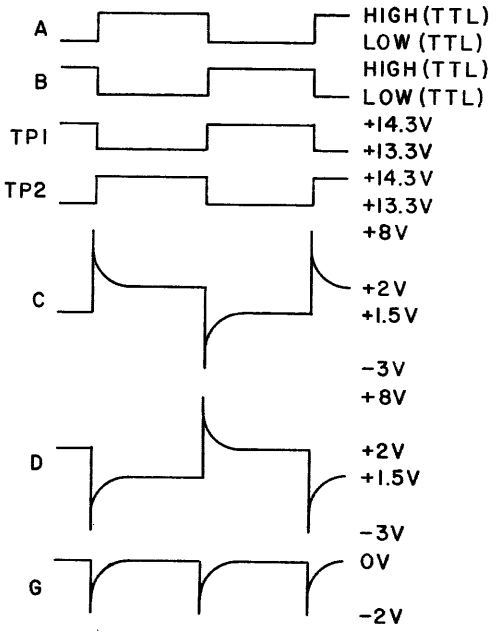
CZJ
Rev A
Sheet 1 of 1

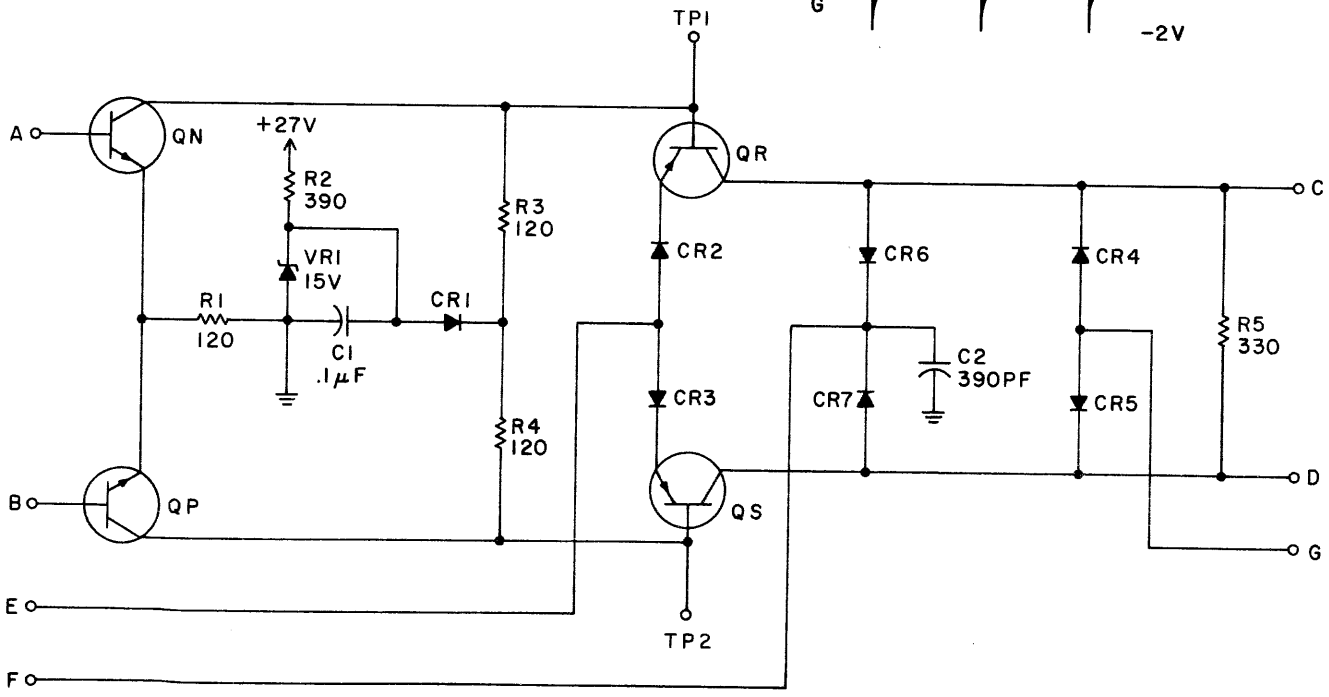
WRITE DRIVER -DLC

The DLC circuit is a differential current switch which converts voltage input signals to current for driving a differential recording head.

TTL level signals are applied to inputs A and B. Transistors QN and QP drive the bases of transistors QR and QS to control current to the head. The current source is connected to input E and supplied to the emitters of transistors QR and QS through diodes CR2 and CR3. Differentiated current is available to the head at outputs C and D. Diodes CR6 and CR7 provide a path to ground for write current when input F is grounded by a write protect circuit. Diodes CR4 and CR5 rectify the echo pulses from the head and apply them to a write voltage fault circuit through output G.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DLC
Rev B
Sheet 1 of 1

Rectifier - DZJ

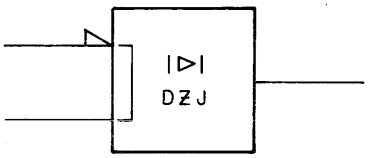
The DZJ circuit is a full wave rectifier with a differential input and single ended output.

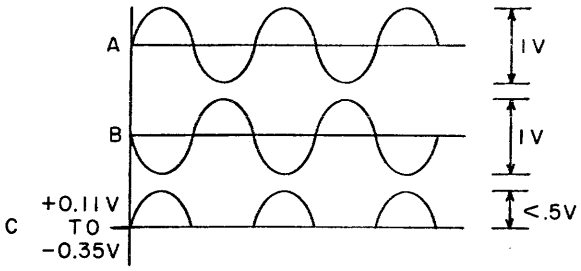
The rectifier consists of a matched pair of transistors (Q1A and B) used as a differential pair. Q1A and Q1B conduct during the positive half input cycle and back biased during the negative half input cycle. Q2 is used as a constant current source supplying about 4.5 ma.

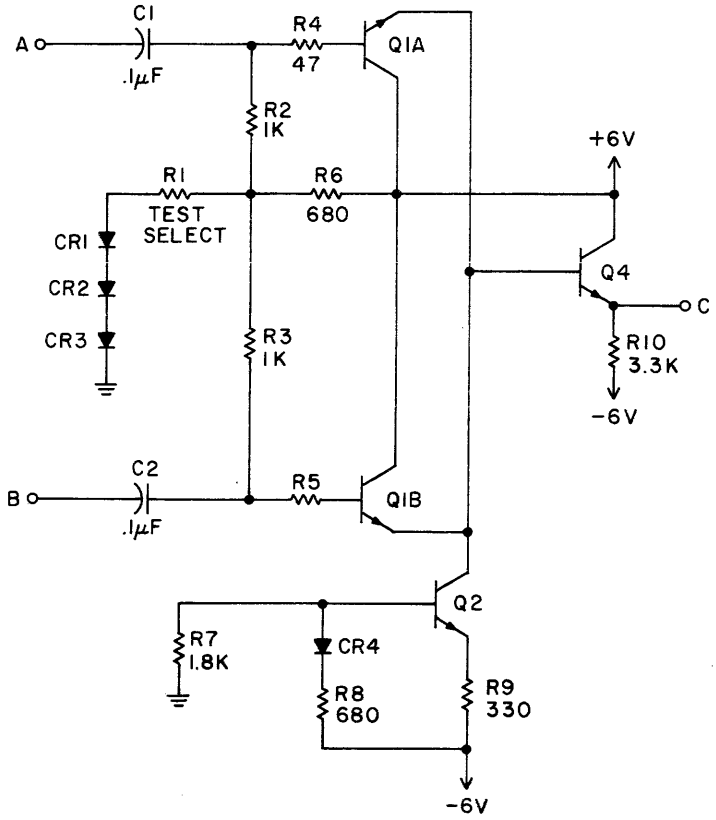
Diodes CR1, 2, and 3 along with test select R1 and R2 form an adjustable bias network. This adjusts the DC base line at output C from about -0.35v to +0.11v and is set so that the output of the AGC amplifier is 2v p-p.

The output buffer amplifier is Q4 and presents a comparatively high input impedance and a low output impedance.

The input frequence response is greater than 2 kHz.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

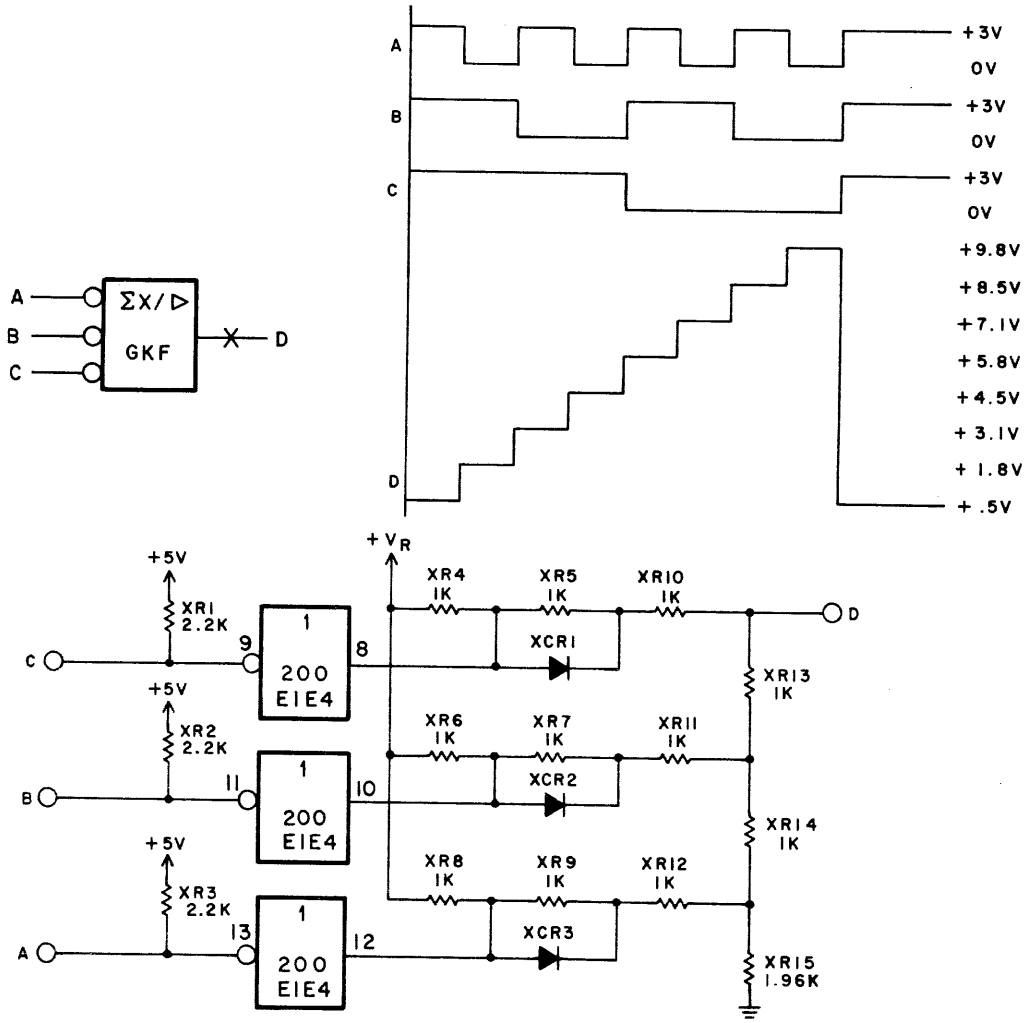
DZJ
Rev A
Sheet 1 of 1

DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_r determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_r is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.



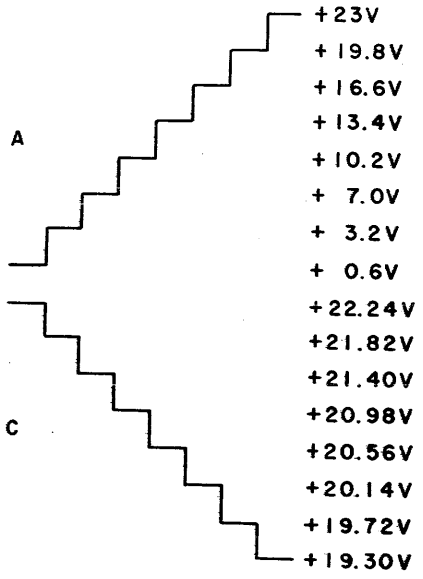
NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY. 7J14

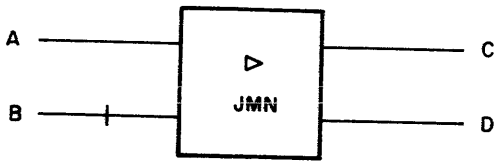
GKF
Rev A
Sheet 1 of 1

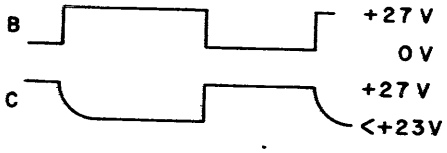
VOLTAGE CONTROLLED CURRENT SOURCE - JMN

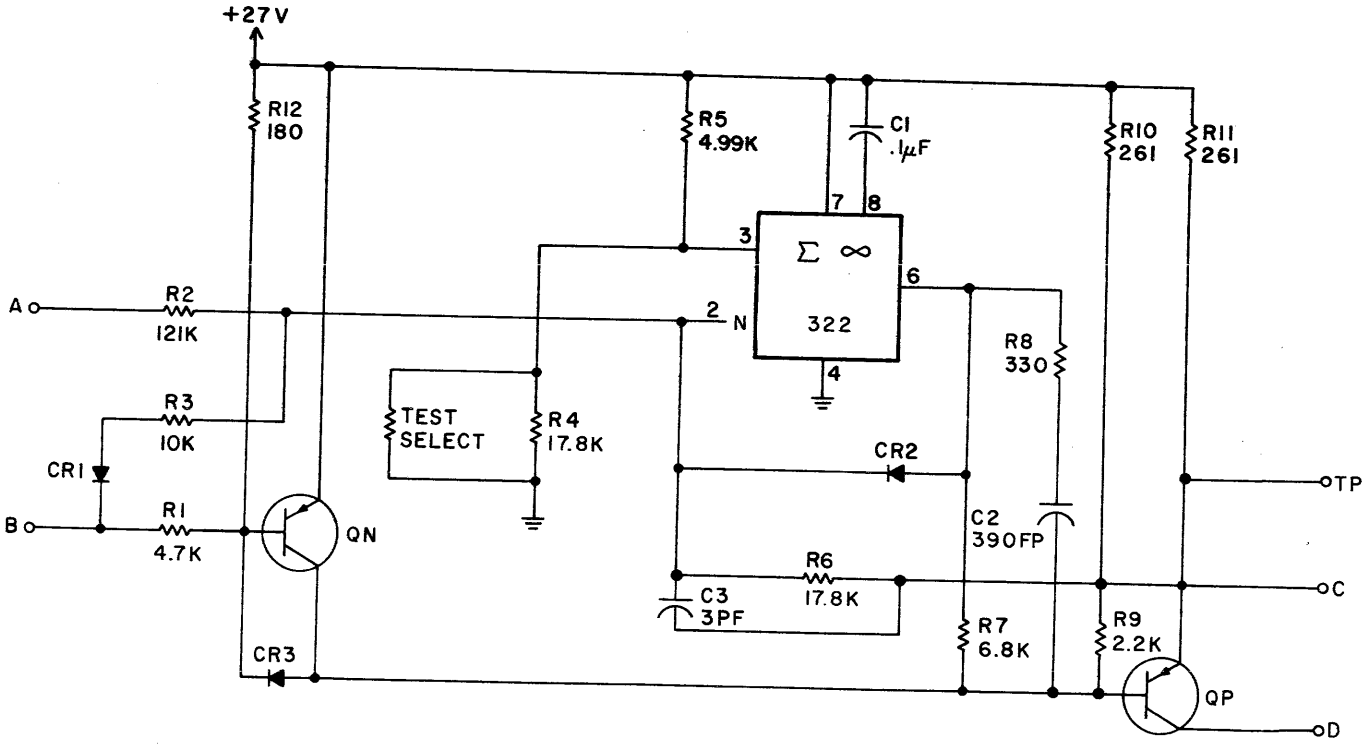
The JMN circuit accepts an analog input voltage and converts it to a voltage controlled current for the write driver.

The JMN circuit receives the analog output of a digital to analog converter. The 322 operational amplifier in the JMN circuit inverts the analog input at A and translates the voltage level to drive the base of current source transistor QP. Write current output is supplied at output D. Current sensing is provided at output C so that other circuitry can test for proper current level output. Control from a write current protect circuit is applied to input B. Current is supplied at output D when input B is +27V. Current source transistor QP is shut off when input B goes to ground.





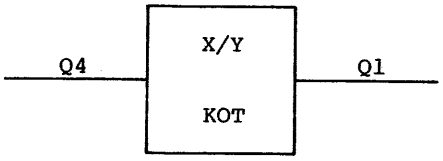


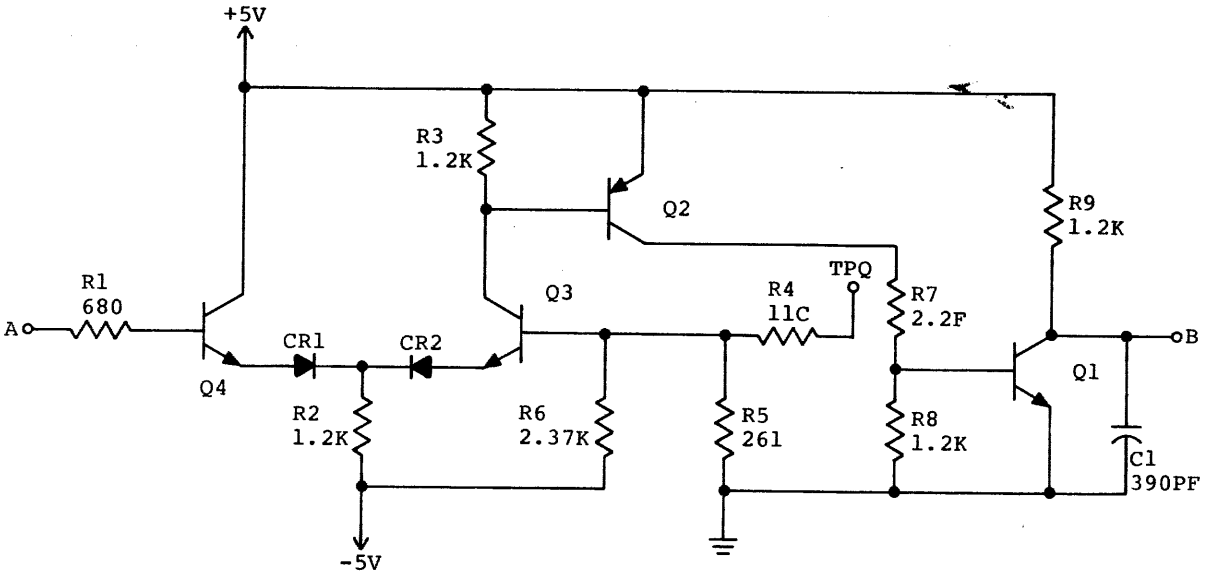


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

JMN
Rev B
Sheet 1 of 1

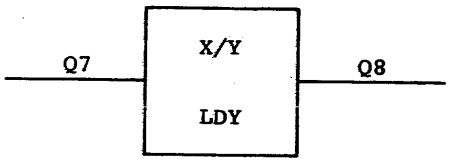
Circuit functional description will be included in a later revision.

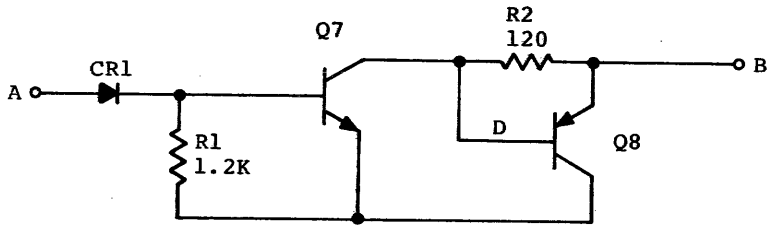




KOT
Rev A
Sheet 1 of 1

Circuit functional description will be included in a later revision.

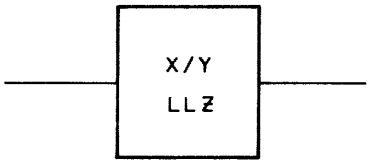


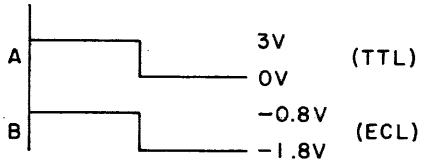


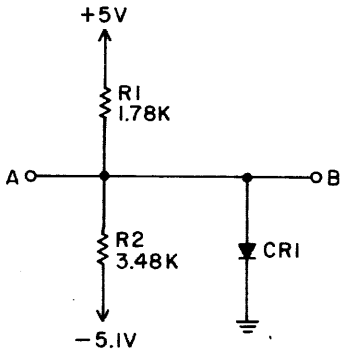
LOY
Rev A
Sheet 1 of 1

PASSIVE TRANSLATOR (TTL TO ECL) - **LLZ**

R3 and R2 form a resistor divider that changes normal (and worst case) TTL levels into normal (and worst case) ECL levels. A "1" TTL will translate into a "1" ECL. R1 serves as a pullup in case there is no input and causes a "1" to be outputted. CR1 is a germanium clamp to limit the output voltage to +0.2 in case an input voltage of +5 or greater is applied.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

LLZ
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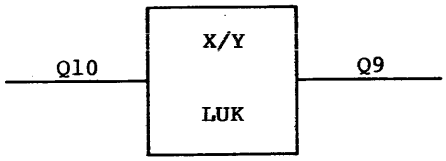
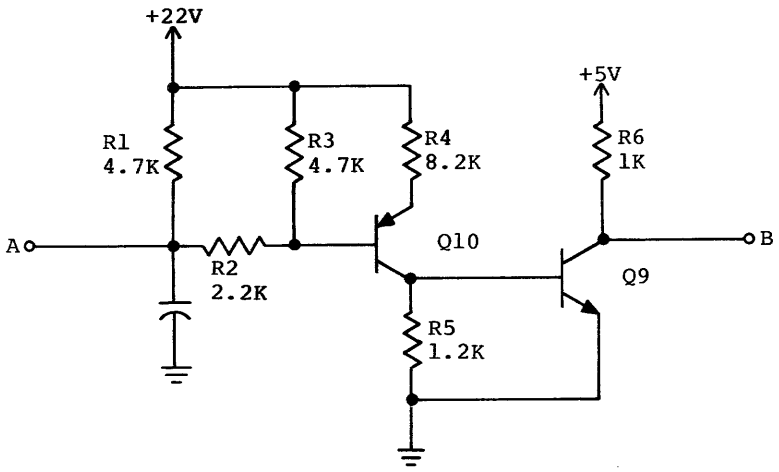
Sheet 1 of 1

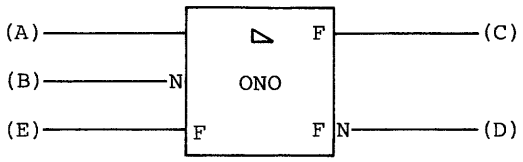
Circuit functional description will be included in a later revision.

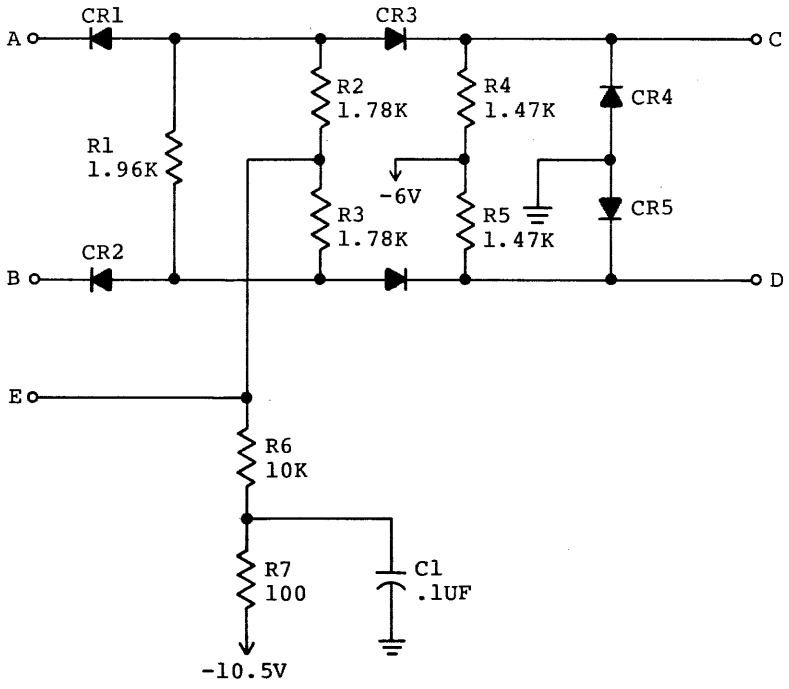




LUK
Rev A
Sheet 1 of 1

Circuit functional description will be included in later revision.

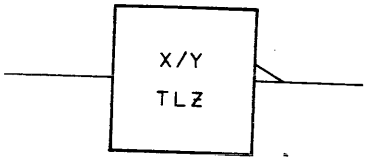


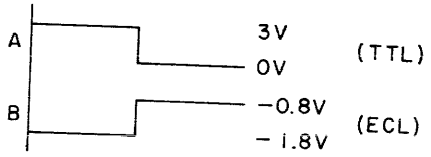


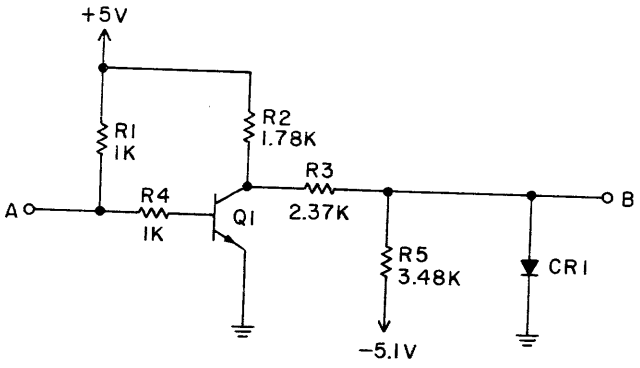
ONO
Rev A
Sheet 1 of 1

INVERTING TRANSLATOR (TTL TO ECL) - TLZ

The first part, consisting of R_1, R_4 and Q_1 form a simple transistor inverter to turn TTL "1's" into TTL "0's". The second part, R_2, R_3, R_5, and CR_1, form a LLZ passive translator which produces ECL levels from TTL inputs.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

TLZ
Rev A
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DELAY - UBD/UBE/UBF/UBH/UBL

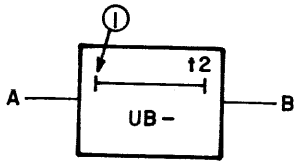
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

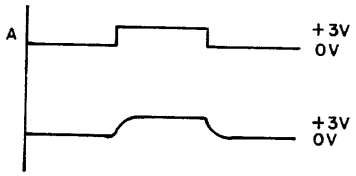
Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

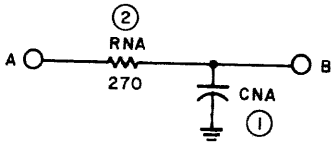
If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay Type	Time
UBD	200 nsec
UBE	0.5 ms
UBF	0.2 ms
UBH	100 nsec
UBL	25 nsec







NOTES:

(1) VARIES WITH TYPE

(2) NOT USED ON UBF AND UBL

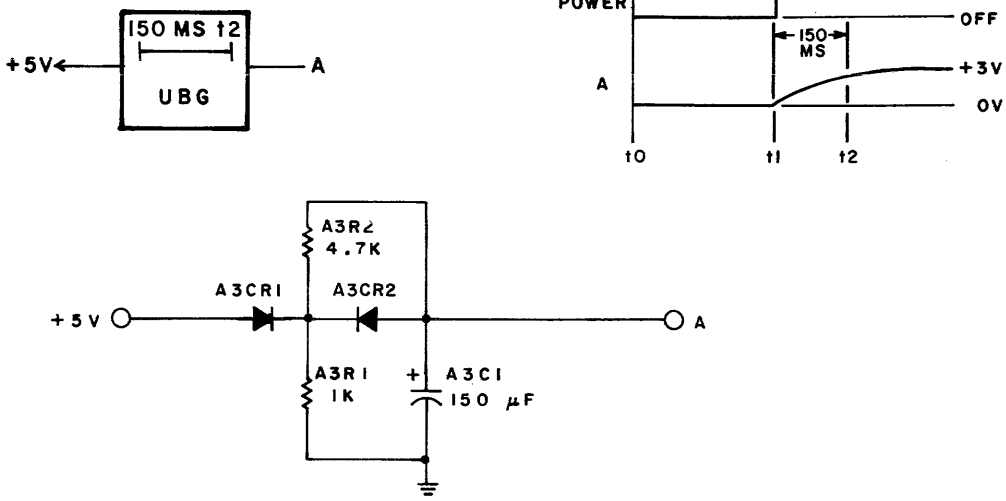
UB-
Rev B
Sheet 1 of 1

DELAY - UBG

The UBG circuit is used to delay application of +5 volts during a power up sequence. Output A drives a standard TTL gate (element number 140).

During a power off phase (t_0), capacitor A3C1 is discharged. When power is applied (t_1), input A is still below the turn-on threshold of the TTL gate due to the discharged state of A3C1. However, the capacitor begins charging through A3CR1, A3R2 and the input resistance of the TTL gate. At time t_2 the capacitor voltage reaches the turn-on threshold of the TTL gate (approximately 1.5v). The capacitor then continues to charge to full capacity.

When the +5 voltage is removed, A3C1 discharges through A3CR2 and A3R1 returning circuit output A to a level below the turn-on threshold of the TTL gate.



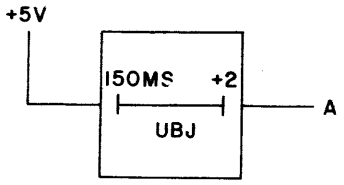
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7337

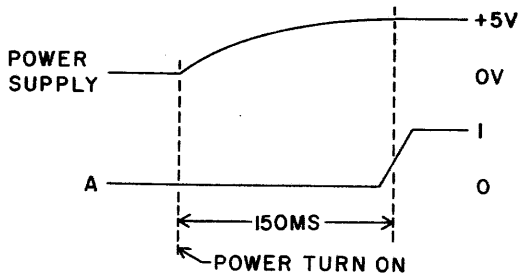
UBG
Rev A
Sheet 1 of 1

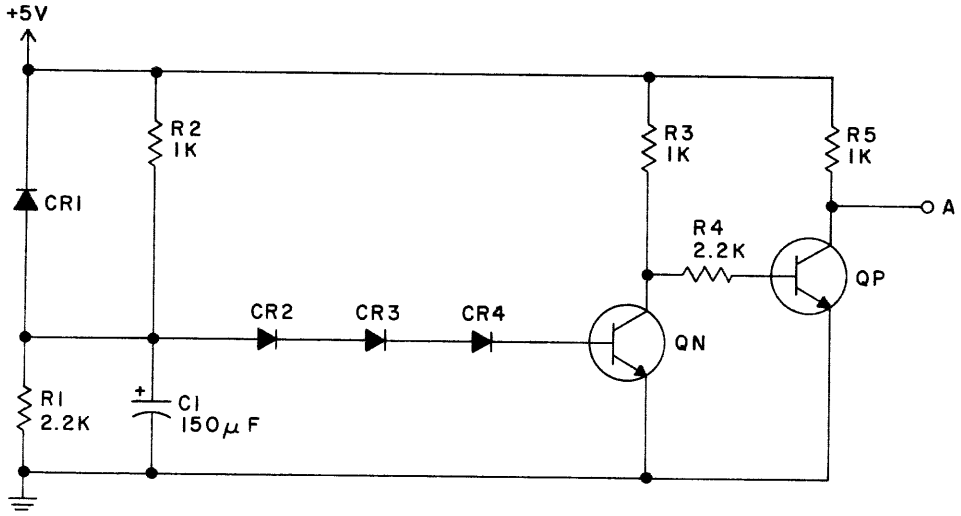
DELAY - UBJ

The UBJ circuit delays application of a "1" to a standard TTL circuit after power is applied.

When power is applied to the UBJ circuit, C1 is charged through R2. After approximately 150 ms from initiation of power-up transistor QN is turned on and transistor QP is turned off, providing a TTL level "1" at output A.







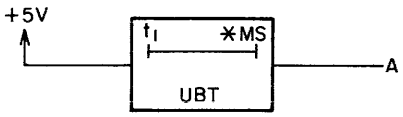
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

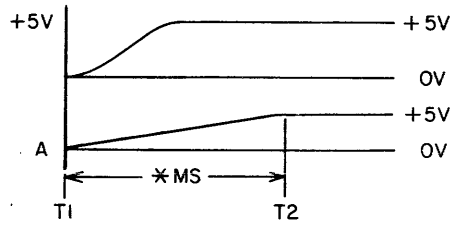
UBJ
Rev A
Sheet 1 of 1

DELAY - UBT

The UBT delay circuit delays application +5 volts to a standard TTL gate during a power up sequence.

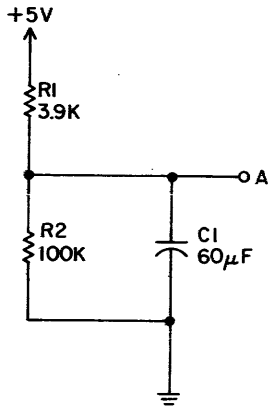
Applying +5v (T1) slowly raises output A to +5 volts as C1 is charging. As the voltage across C1 approaches 5 volts, output A raises to 5 volts after a specific delay time determined by the values of R1, R2, and C1.





* TYPICAL DELAY TIMES

R1	R2	C1	DELAY TIME
3.9K	100K	60μF	80 MS
6.8K	10K	60μF	30 MS



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UBT
Rev A
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DELAY - UC-

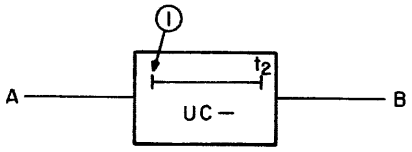
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v and a capacitor connected to ground.

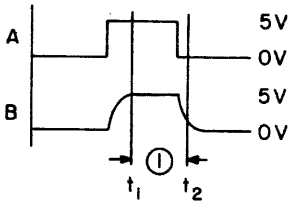
Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

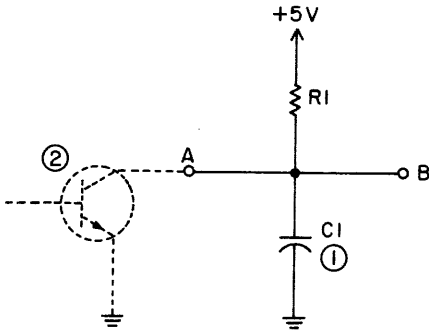
If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

Circuit Type	Capacitance	Resistance	Delay
UCM	5600PF	1.2K	1.5US
UCP	5600PF	560	0.8US
UCR	5600PF	1K	1.3US
UCS	3.3UF	2.2K	1MS
UCV	270PF	2.61K	175NS
UCY	200PF	10K	200NS







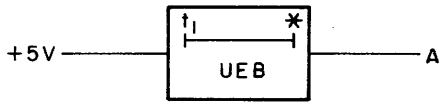
NOTES:
① DELAY TIME DEPENDENT ON CIRCUIT TYPE.
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

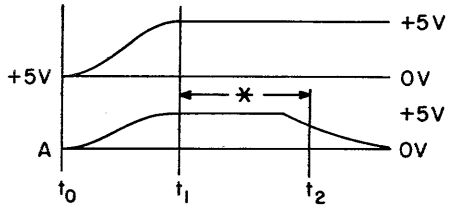
UC-
Rev B
Sheet 1 of 1

DELAY - UEB

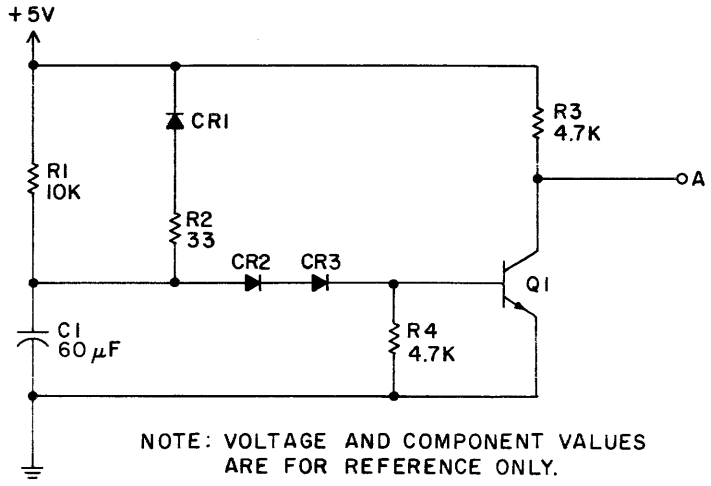
The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor C1 is discharged by R4, CR2, and CR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and C1 is charging. As the voltage across C1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.





* DELAY TIME VARIES WITH COMPONENT VALUES, SEE LOGIC DIAGRAMS FOR SPECIFIC DELAY TIME.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

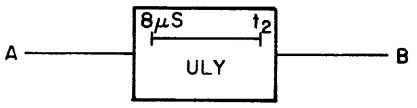
UEB
Rev A
Sheet 1 of 1

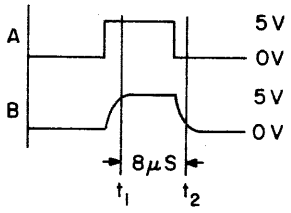
DELAY - ULY

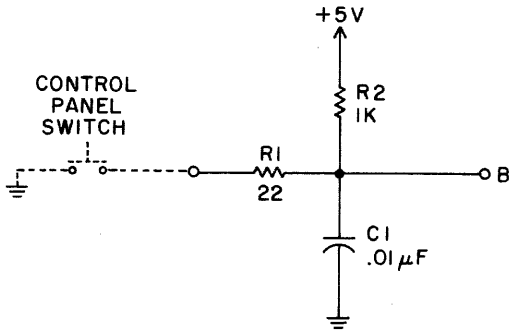
The ULY-delay circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v, a capacitor connected to ground, and a series input resistor.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If an open circuit ("1") enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.







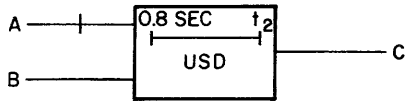
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

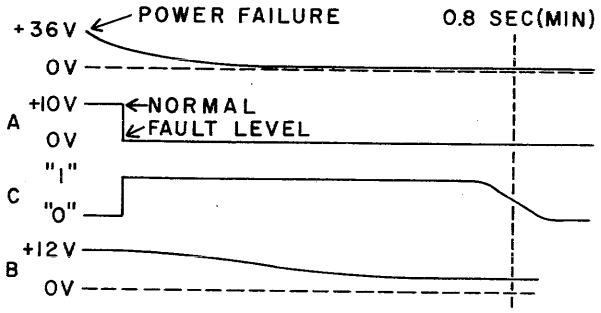
ULY
Rev A
Sheet 1 of 1

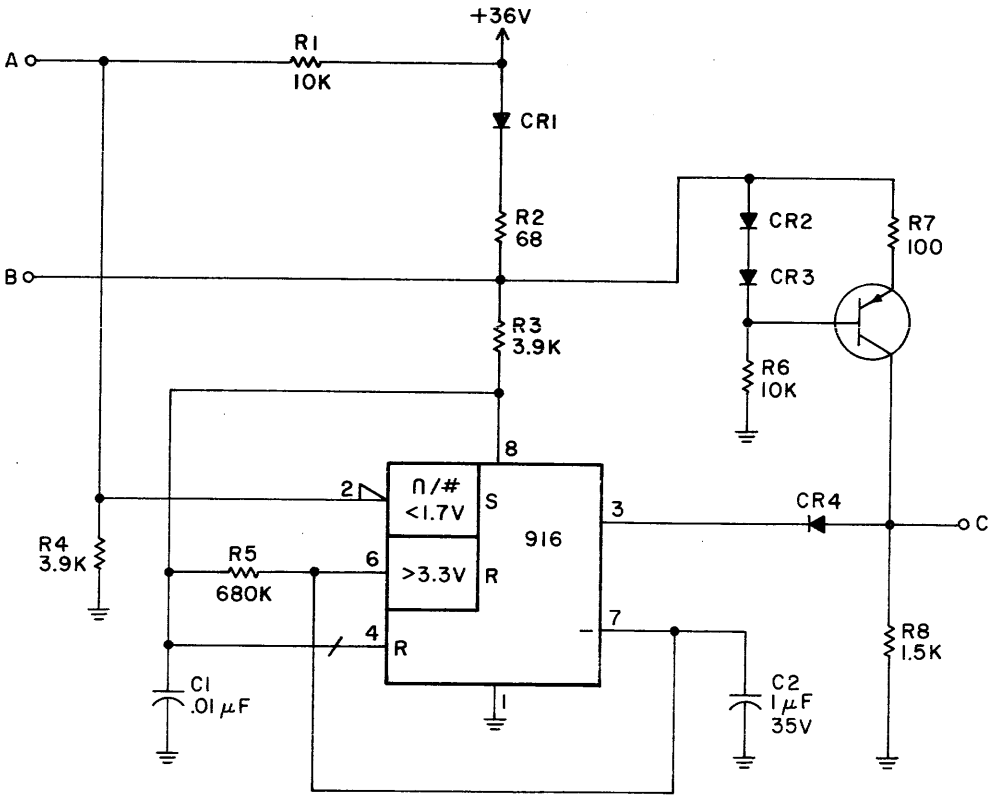
DELAY - USD

The USD circuit maintains a TTL high level output for 0.8 sec during the time that the power supply voltage is dropping.

The USD circuit functions as the delay portion of a write fault clamp circuit which prevents write current from reaching the head during a +36 V supply voltage fault condition. The switching action of transistor QN is initiated by the fault trigger at input A. QN is turned on when input A goes to 0 V, causing output C to go high. Resistor R5 and capacitor C2 provide the time-out constant to keep output C high for 0.8 sec. Stored energy is supplied at input B to maintain QN in the on state for the 0.8 sec duration. The high output at C is used to switch on a write clamp circuit.



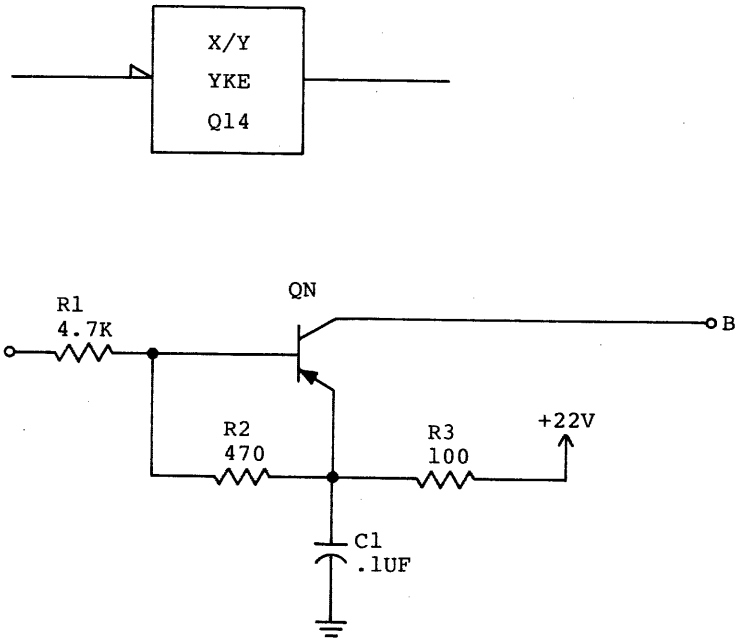




NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

USD
Rev B
Sheet 1 of 1

Circuit functional description **will be included** in later revision.



YKE
Rev A
Sheet 1 of 1

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